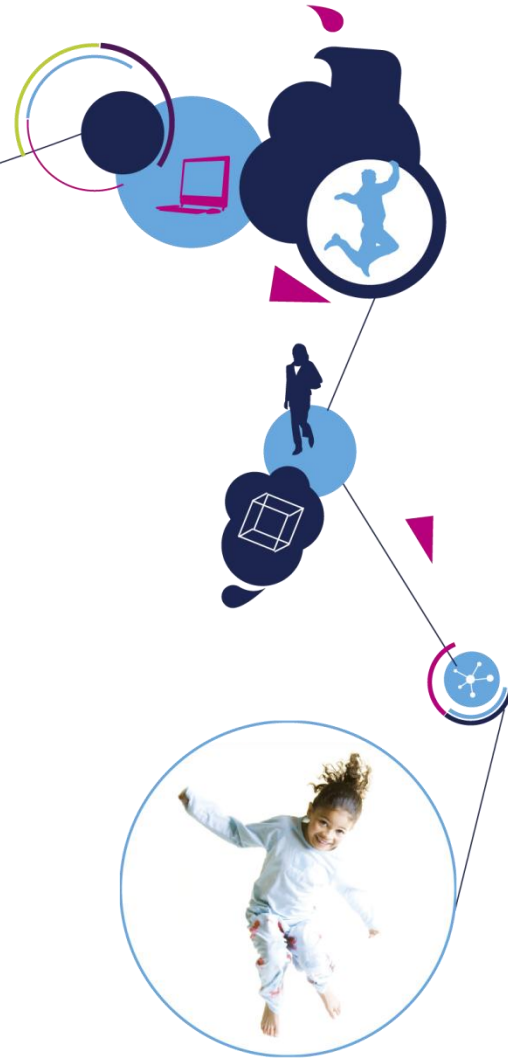
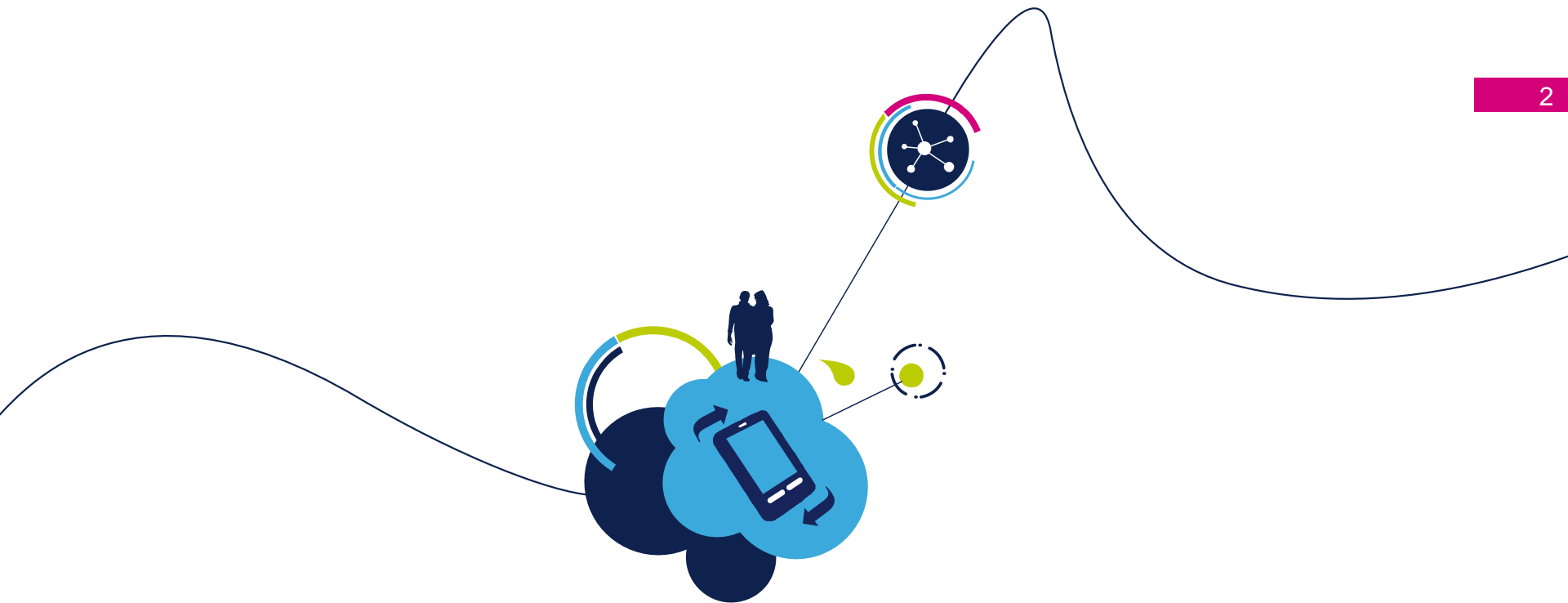




Manufacturing and Technology R&D

Jean-Marc Chery
Executive Vice President
Chief Manufacturing and Technology Officer





1. Introduction

Complete Products, IPs, & Technologies Portfolio

3

Power management



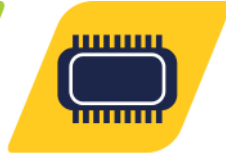
MEMS sensors



Analog



MCUs / ASICS



Automotive



Imaging



Smartphones and tablets



TV & digital set-top box



Power & Discrete

MEMS

BCD

eNVM

Analog Mixed Signal/RF

Advanced CMOS

Leadframe package leaded / leadless

MEMS

Leadframe package leaded / leadless

Laminated substrate package wired

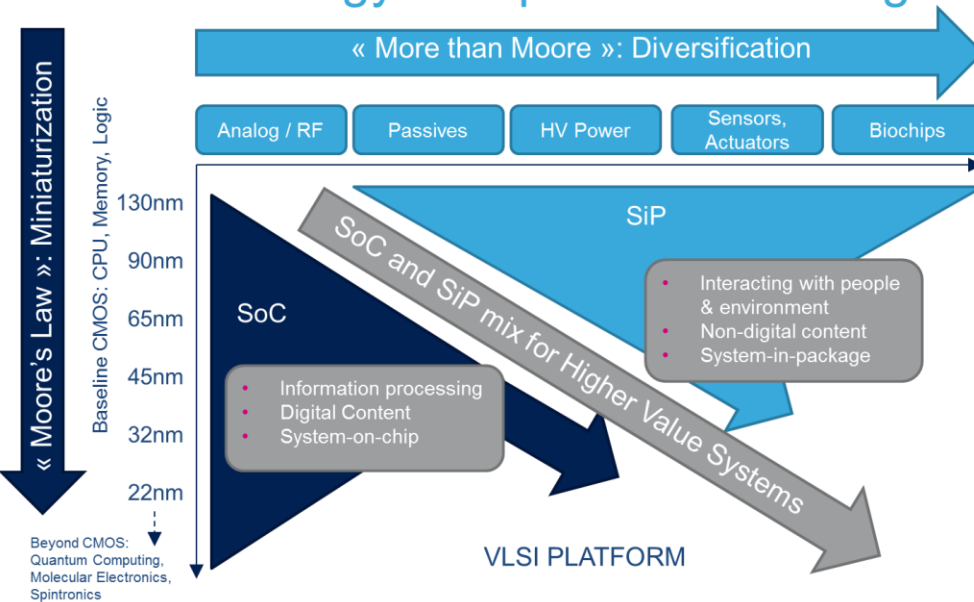
Laminated substrate package flipchip

WLSP & 3D Integration

Technology R&D Model

4

Technology Competitive Advantage



CMOS Technology Alliances



Pre T0 Alliance: Advanced R&D

- 14nn Finfet
- FDSOI

ISDA: Bulk/low-power (LP) technology

- 32/28nm
- 20nm

* Renesas is only part of the Pre T0 Alliance

Technology R&D Model

5

Technology Competitive Advantage

« More than Moore »: Diversification

Analog / RF

Passives

HV Power

Sensors,
Actuators

Biochips

SoC

- Information processing
- Digital Content
- System-on-chip

SiP

- Interacting with people & environment
- Non-digital content
- System-in-package

SoC and SiP mix for Higher Value Systems

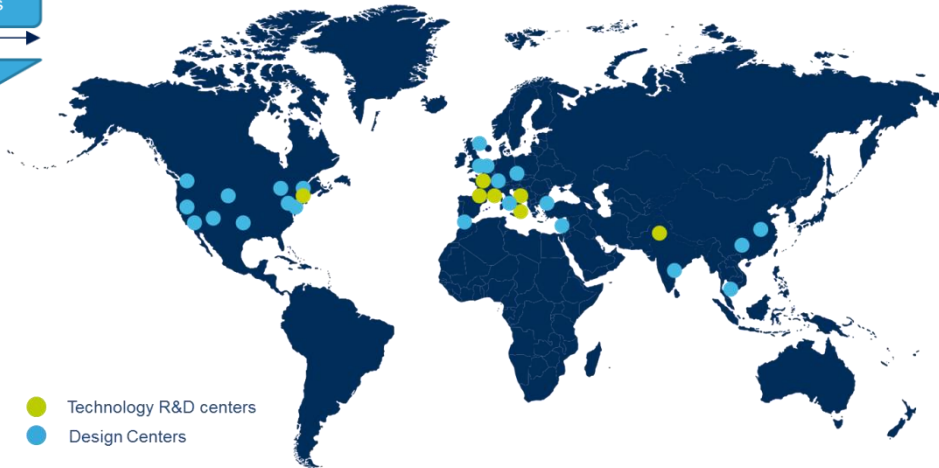
VLSI PLATFORM

An Unwavering Commitment to R&D

7 main technology R&D centers

39 design centers – 20,000 patents

12,000 people in technology, design, product and system R&D



« Moore's Law »: Miniaturization

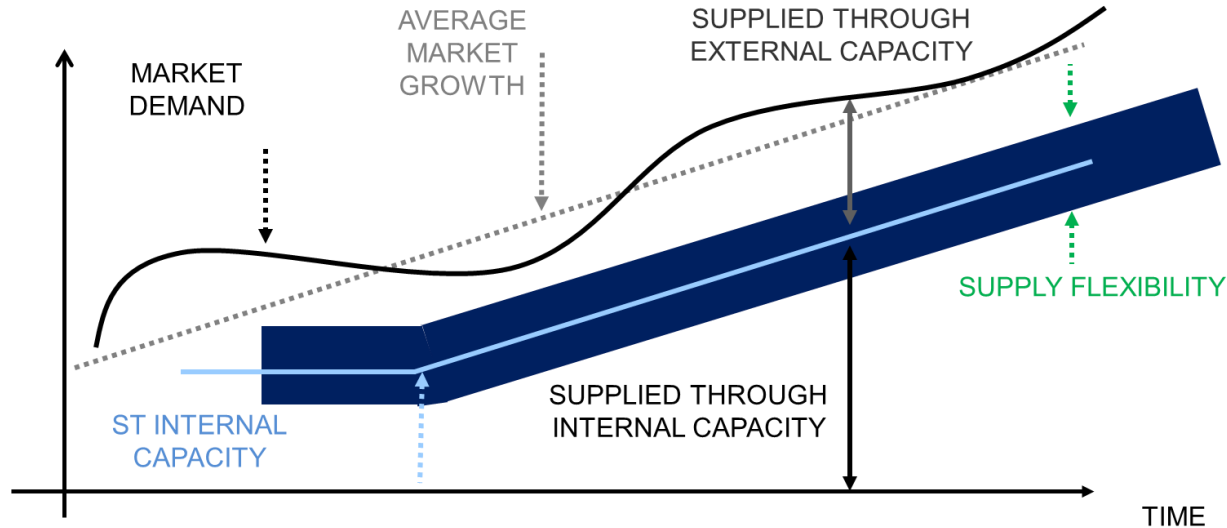
Baseline CMOS: CPU, Memory, Logic

130nm
90nm
65nm
45nm
32nm
22nm

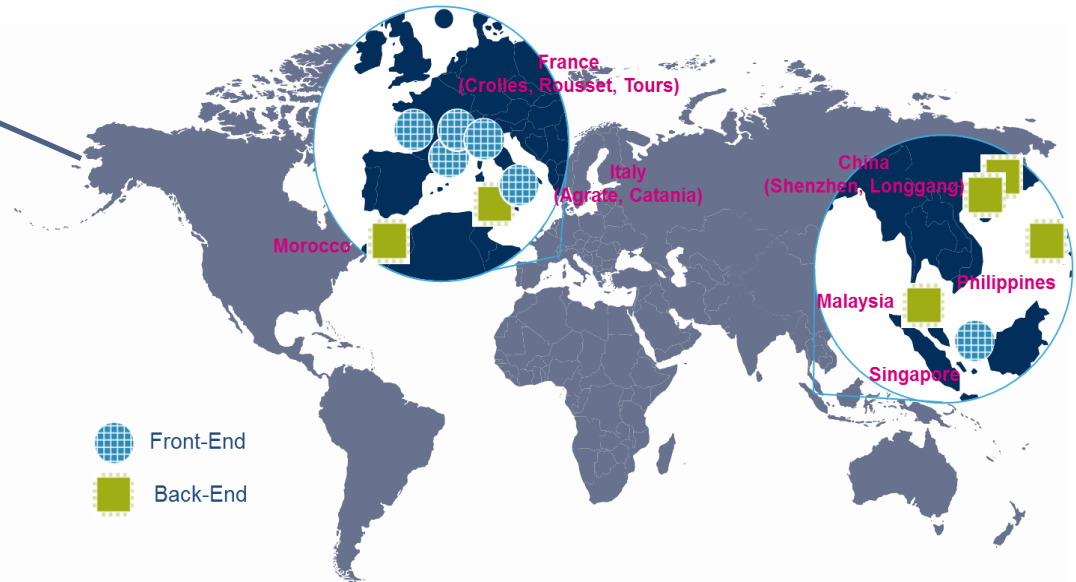
Beyond CMOS:
Quantum Computing,
Molecular Electronics,
Spintronics

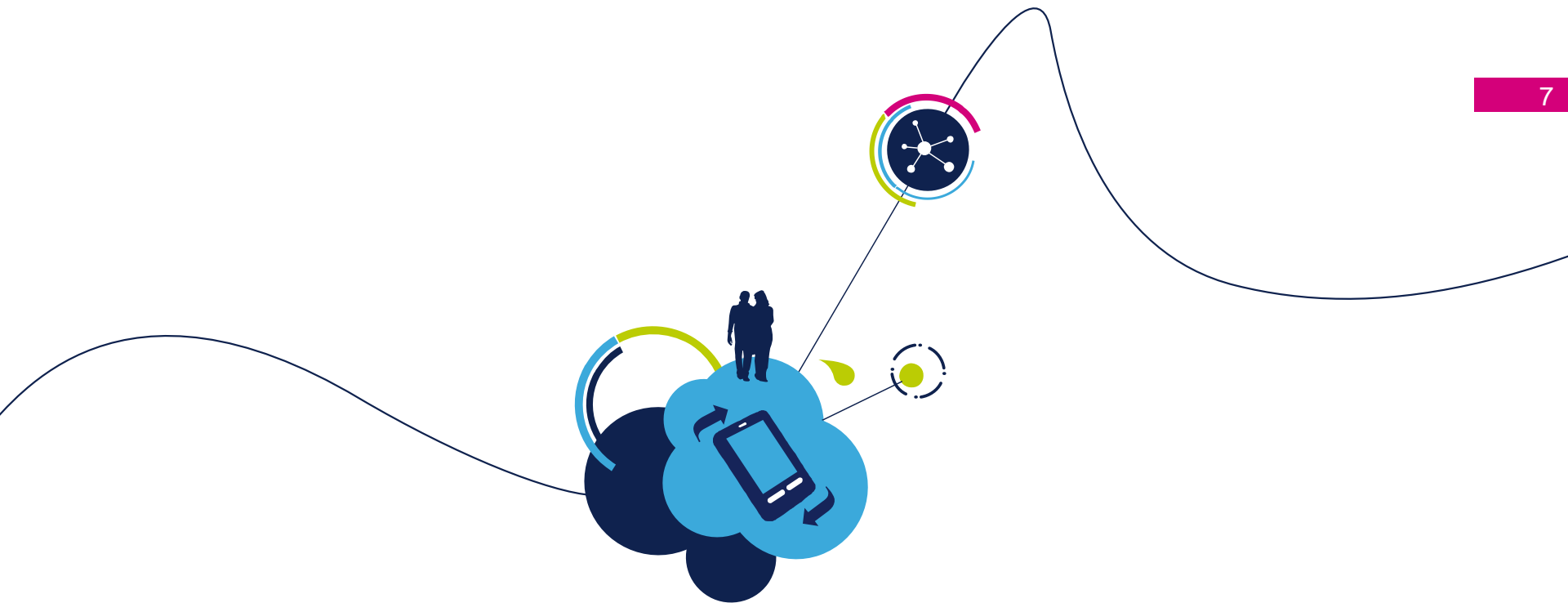
Manufacturing Model

6



Flexible and independent manufacturing





2. Technology R&D

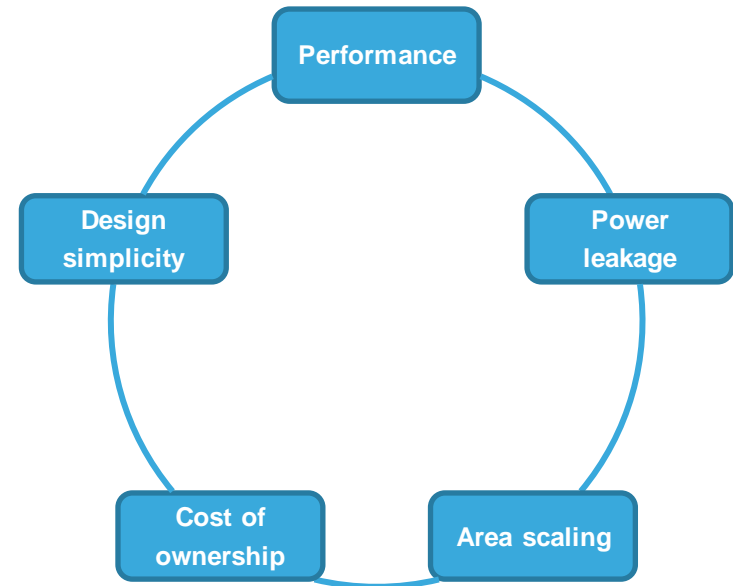
Multimedia Convergence: The Ideal Technology

8

Multimedia convergence is about...

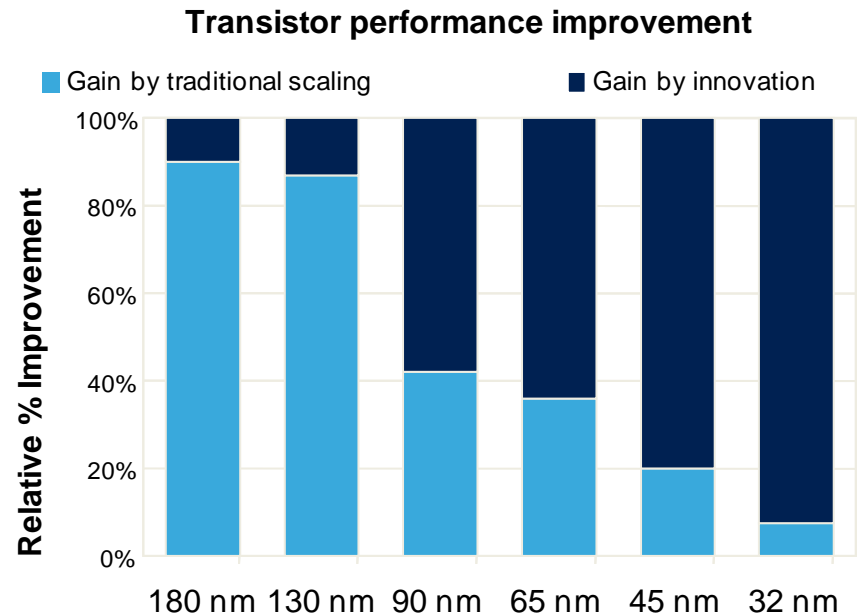
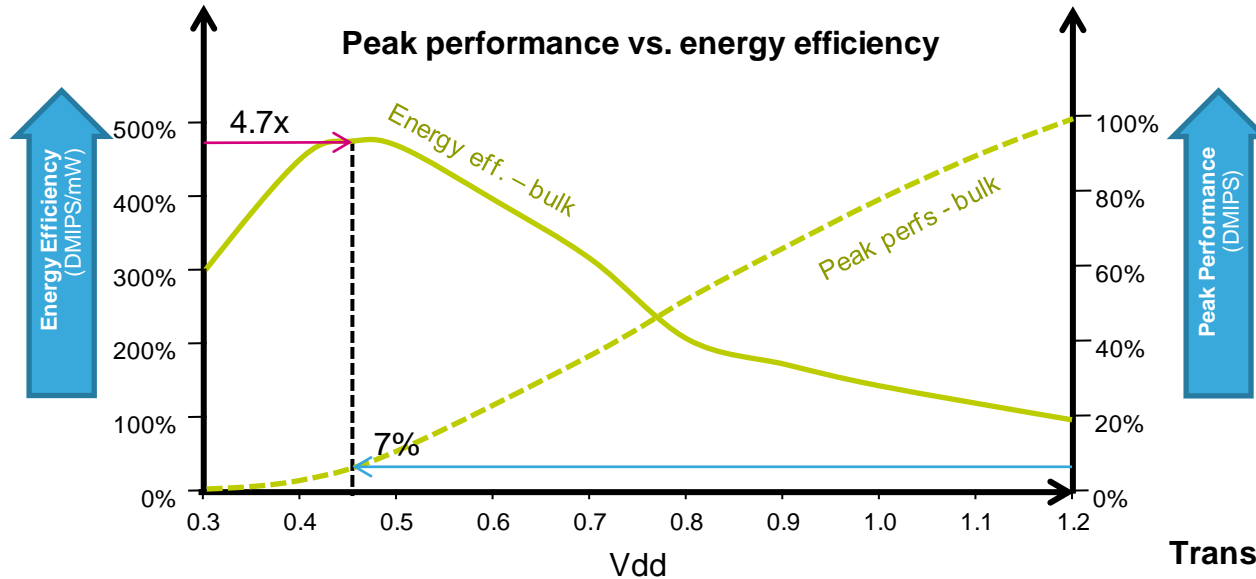


- Cloud (link between Network and Consumer equipment)
- Home servers and Gateways
- Connected Clients (OTT, Android, HTML5)
- Multi-screen, multi-application



Multimedia Convergence: 28nm Bulk Weaknesses

9

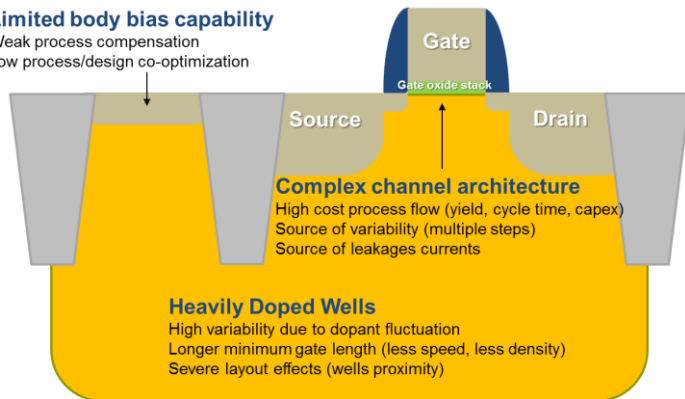


Multimedia Convergence: Fully Depleted Devices Enabling sub-20nm Technologies

10

- Main candidates after bulk are fully depleted devices
 - For improved electrostatic control and device scalability

Limited body bias capability
Weak process compensation
Low process/design co-optimization

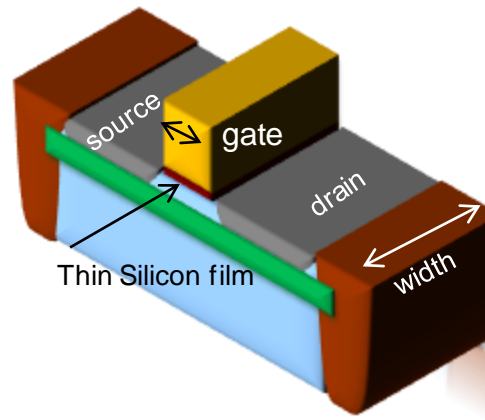


Complex channel architecture
High cost process flow (yield, cycle time, capex)
Source of variability (multiple steps)
Source of leakage currents

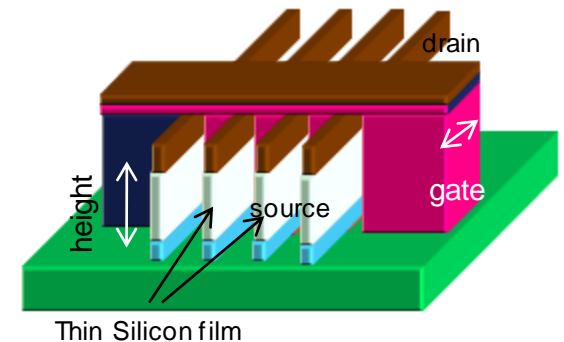
Heavily Doped Wells

High variability due to dopant fluctuation
Longer minimum gate length (less speed, less density)
Severe layout effects (wells proximity)

FDSOI = 2D

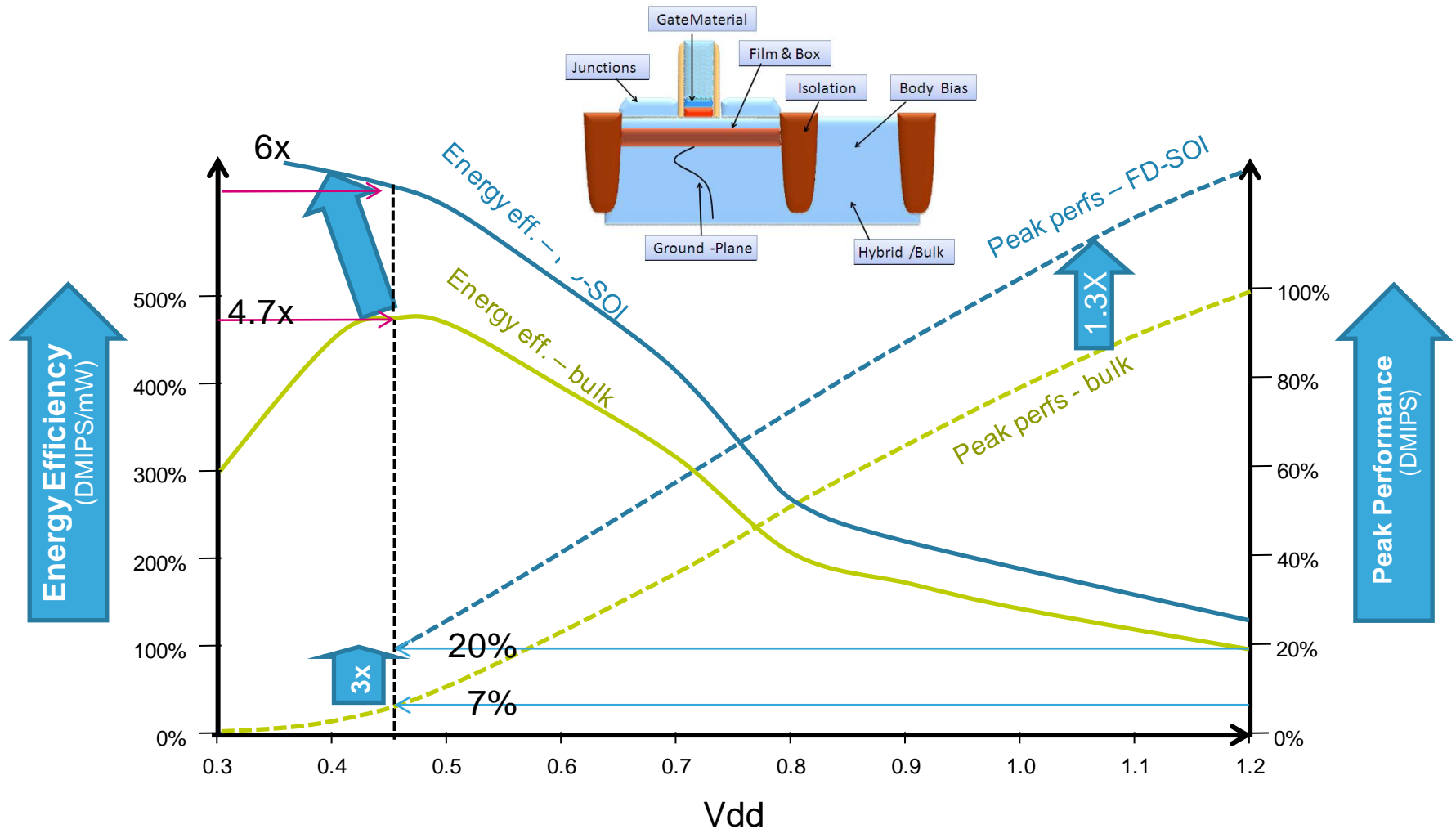


FinFET = 3D



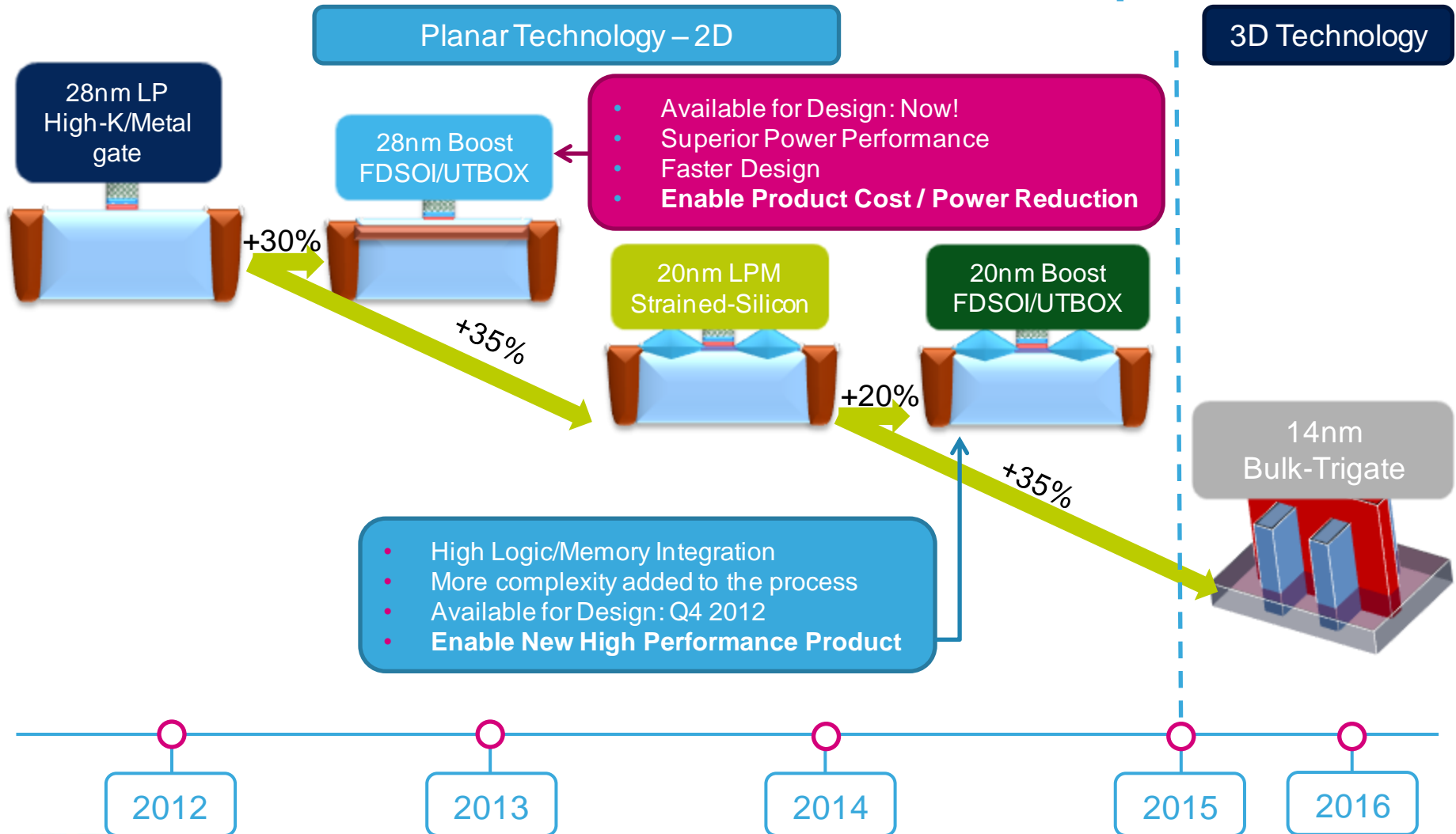
Multimedia Convergence: 28nm FDSOI Better Energy Efficiency

11



Multimedia Convergence: Value Proposition

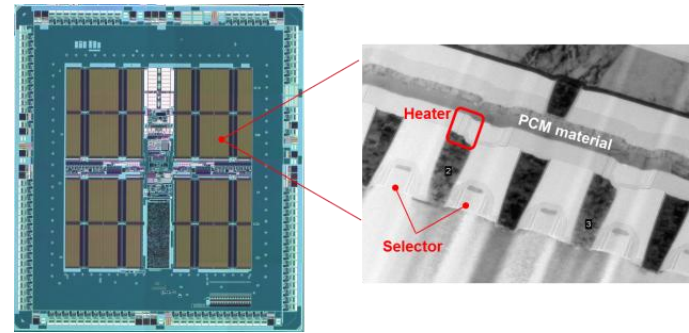
12



Other VLSI Key Differentiation Initiatives

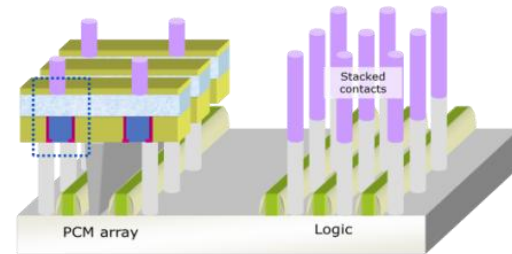
13

- Embedded Flash PCM for future shrink nodes



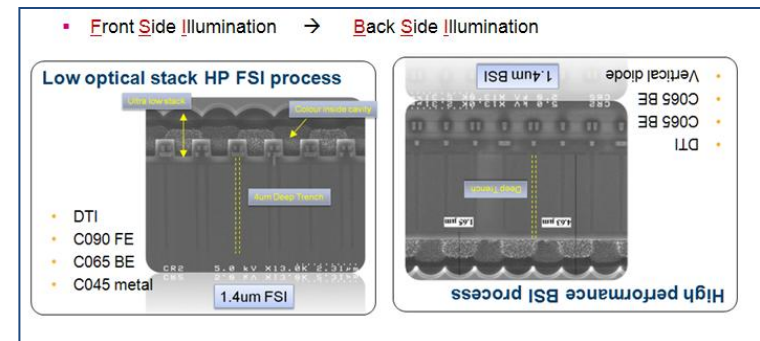
Memory Architecture

- Ultra Fast and Low Power Microcontrollers



A true 3D integration of Non Volatile Memory

- Imaging sensor with BSI on bulk

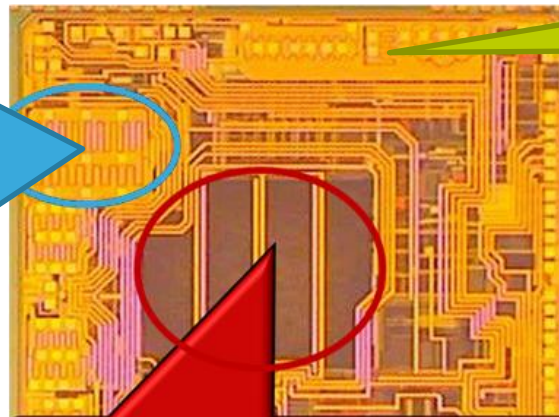


Smart Power: The Ideal Technology

14

POWER DEVICES

- Figures of merit:
 - $R_{sp} = R_{on} \times A$
 - Gate charge (Q_g) – F_{sw} up to 5 Mhz
 - Safe operating area
- Trends:
 - Integration density saturating with LITHO scaling
 - Device architecture and drain engineering
 - Thick copper metallization for high current



- Thick Cu metallization & bonding over active areas

ISOLATION

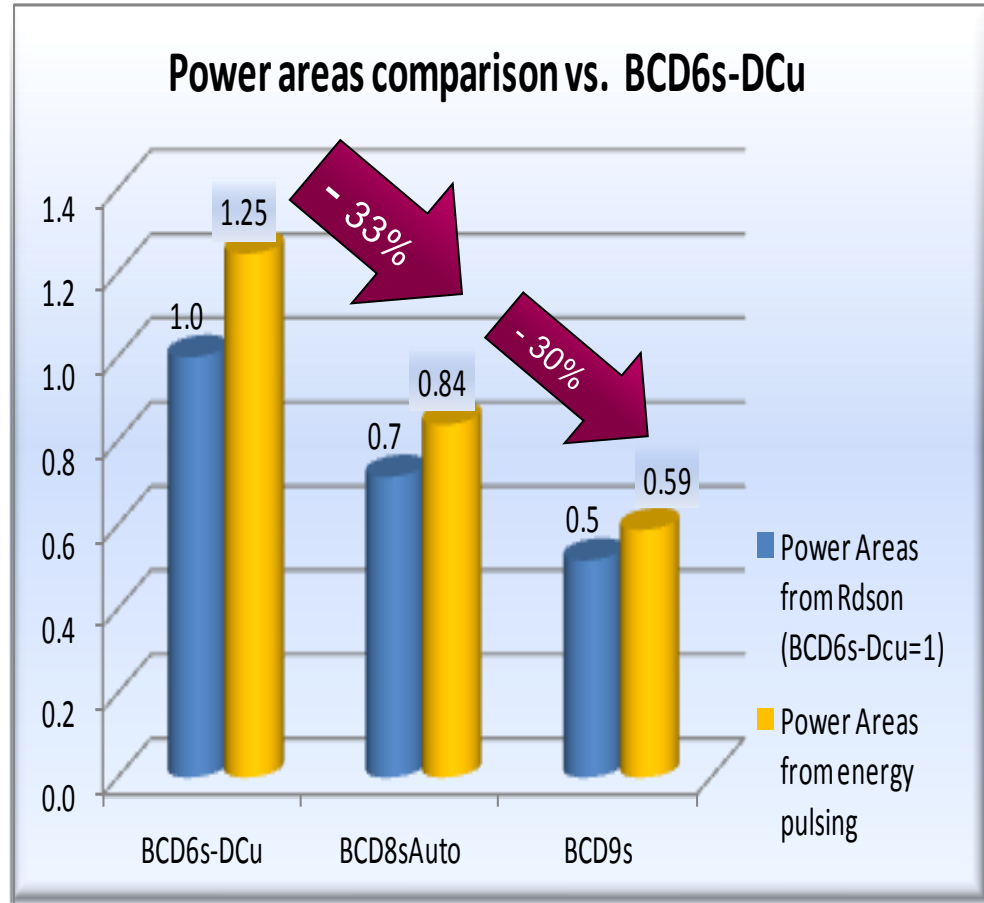
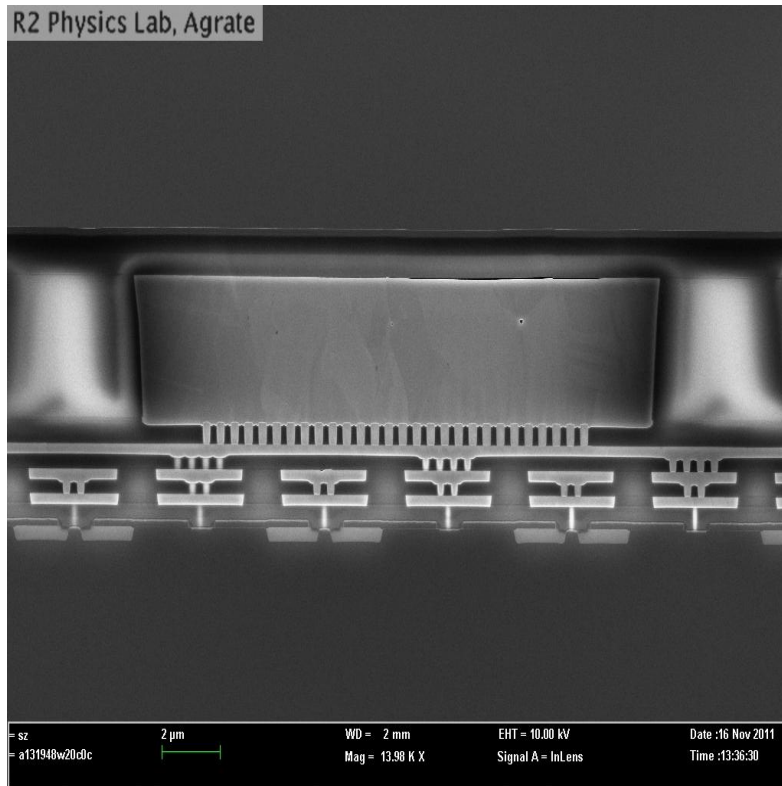
- Junction isolation
- DTI (Deep Trench Isolation)
- SOI

- LOGIC: from 100 K gates up to 500 K gates
- e-Memories

ST ROADMAP

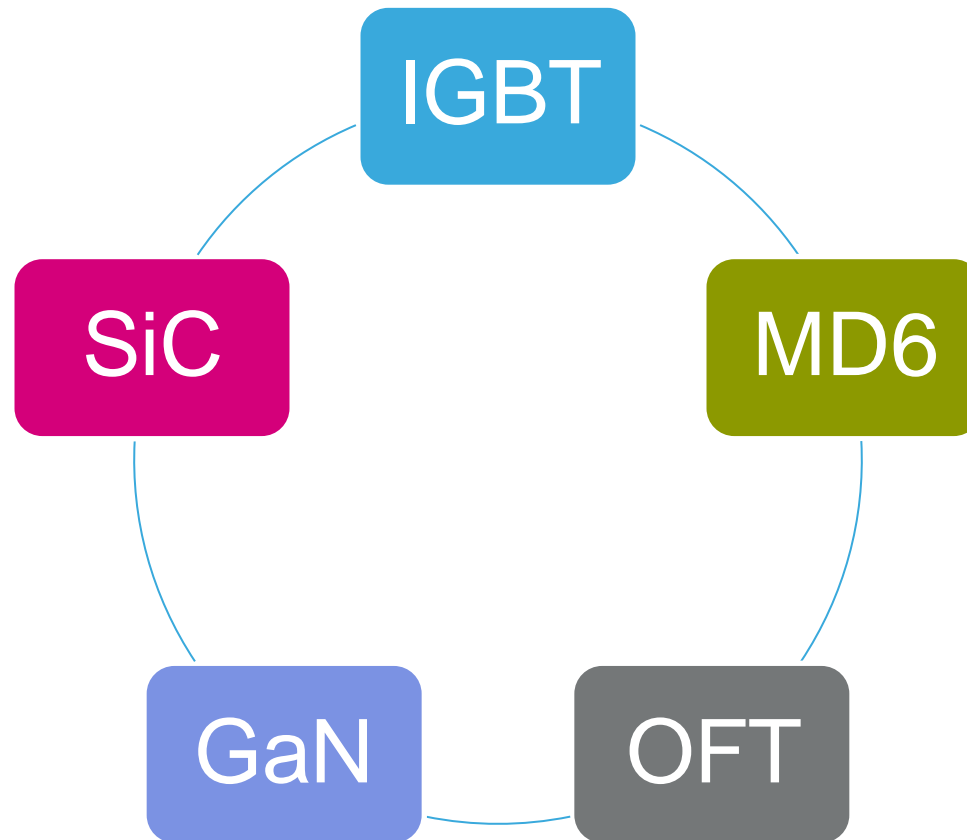
- BCD8sP best in class for Power devices integration capabilities
- Customized solutions by application → Low Maks Count
- BCD9s (110 nm) ready for prototype in Q113 and BCD10 (90 nm) process architectures in definition phase

Full Copper Metallization



POWER: Top Priority Technology Platforms

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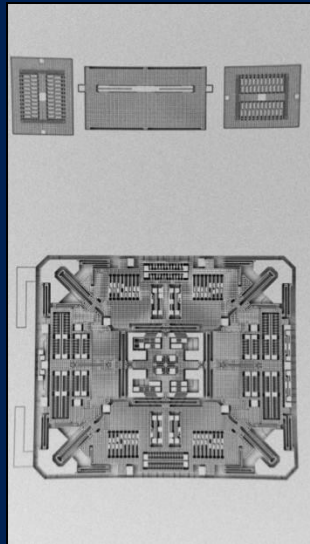
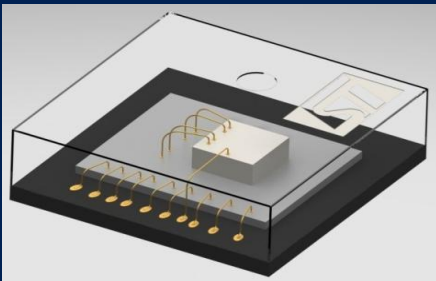


SENSE: Technology Coverage

17

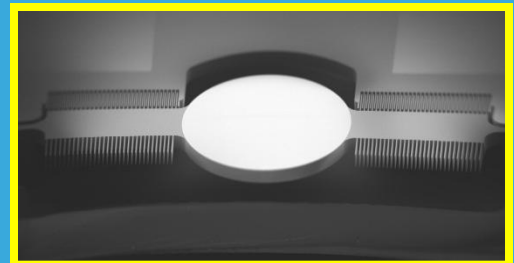
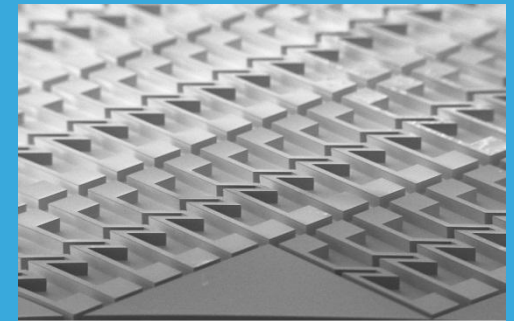
SENSORS

- Accelerometers
- Gyroscopes
- Compasses
- iNEMO™
- Pressure
- MicroPhone



ACTUATORS

- Thermal
- Piezoelectric
- Electrostatic

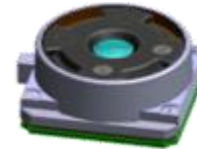
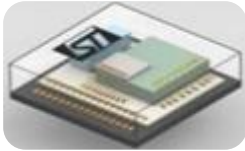


Packaging Technology R&D

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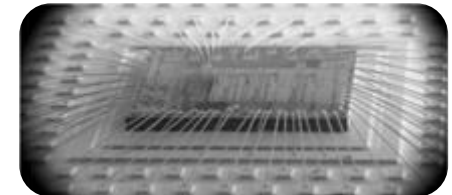
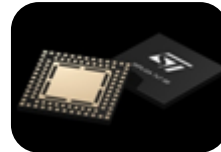
Sense

MEMS and microphones (LGAs), Optical modules and Imagers towards BSI



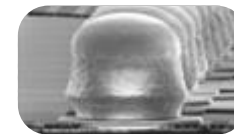
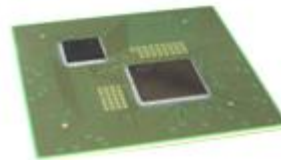
Power & BCD

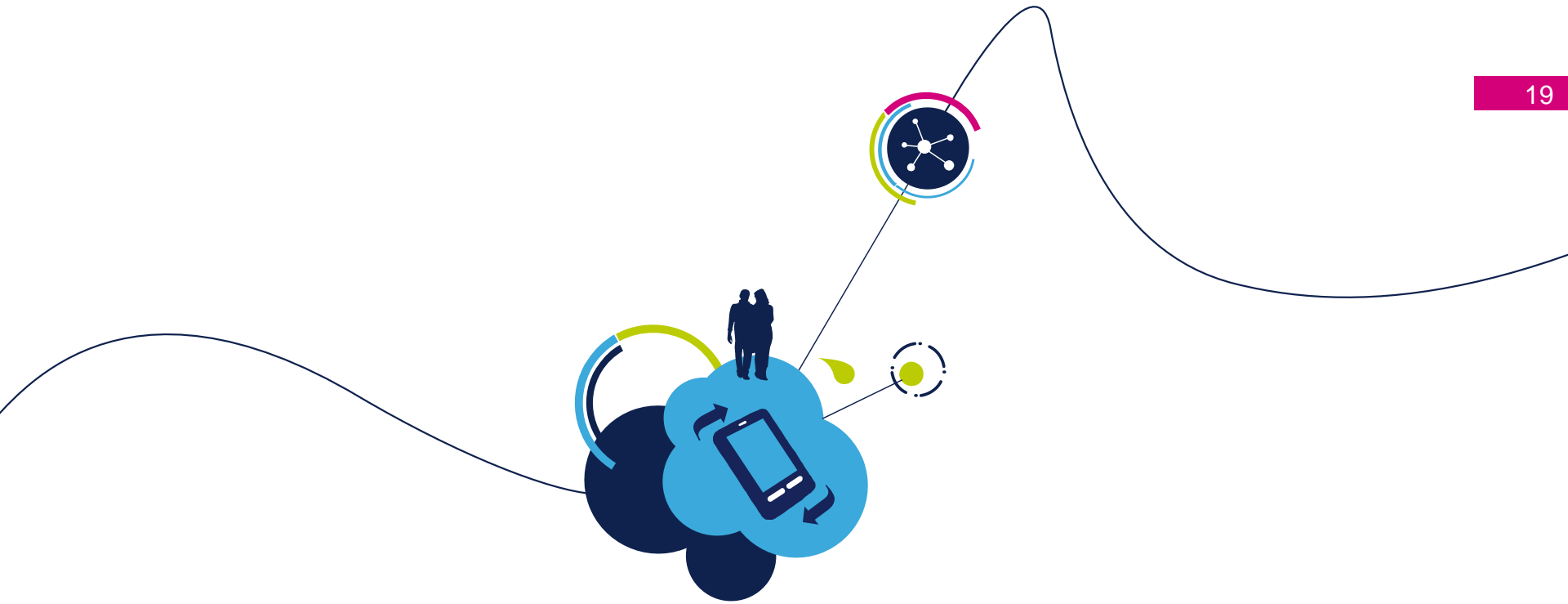
High dissipation, miniaturized packages (PSSO, QFNs)



Multimedia Convergence with advanced CMOS

Integration and miniaturization based on BGAs. Towards Flip Chip & WLP





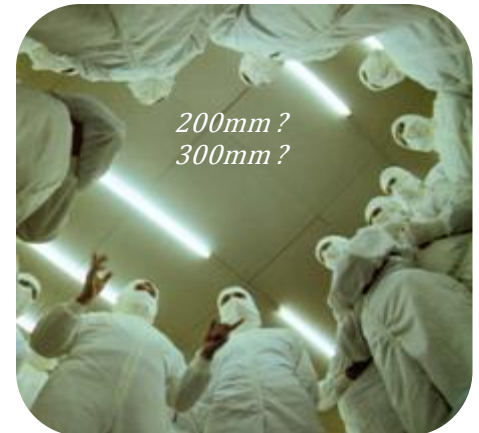
3. Manufacturing

Front-End Manufacturing: Flexibility/Efficiency

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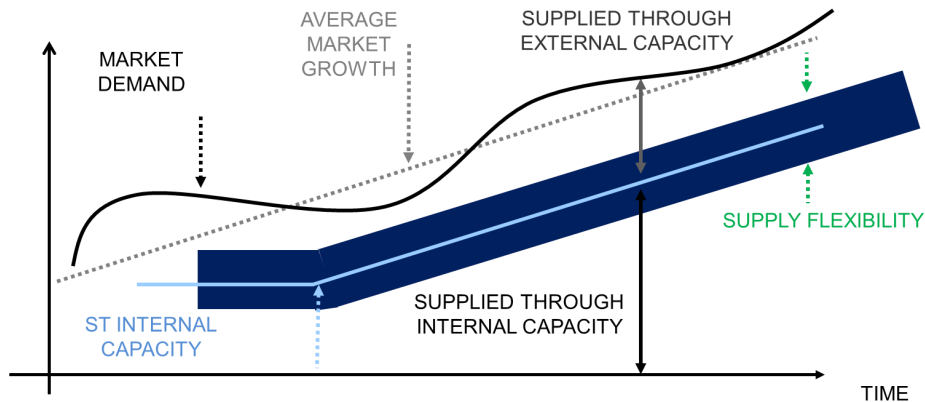
Manufacturing flexibility across market cycle

- Minimize unused capacity in the downturns and lean investment to support upsides:
 - Model deployment by technology cluster better balancing internal vs. external with new major initiatives:
 - Start new generation of BCD (Smart Power) outsourcing
 - Start CMOS 28/20 nm FDSOI outsourcing
 - Start advanced CMOS Imaging Sensor with BSI
- Guarantee in-out flexible sourcing at product level
- Make fixed cost variable wherever possible



Front-End Manufacturing: Outsourcing Map

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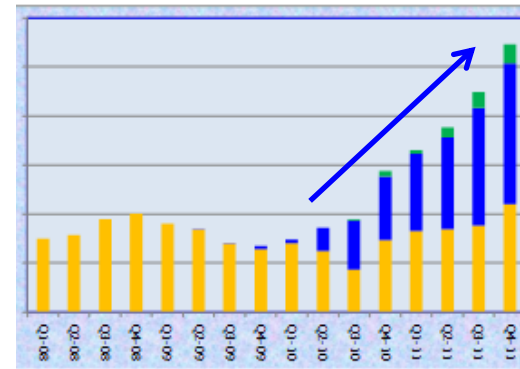
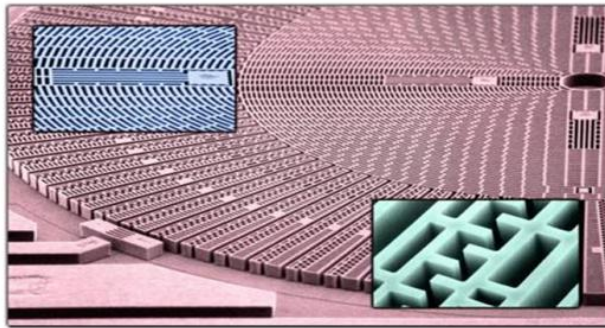
Technology / Source	First: Time to Market	Second	Alternative
CMOS 45LP	Crolles 300	Foundry*	No
CMOS 40LP	Crolles 300	Foundry*	Foundry**
CMOS 32LP	Foundry*	Crolles 300	No
CMOS 28LP	Foundry*	Crolles 300	Foundry**
CMOS 28 FDSOI	★ Crolles 300	Foundry*	No

Technology / Source	First : Time to Market	Second	Alternative
HCMOS9A	Crolles 200 / 300	Rousset 8	Foundry*
CMOS65 / 55RF	Crolles 300	Foundry*	No
CMOS Imaging Sensor	★ Crolles 300	Foundry*	No
CMOS55 eFlash	Crolles 300	Foundry*	No
CMOS M10 / F10 eFlash / eEEPROM	Rousset 8	Foundry*	No
BCD8	★ Agrate 8	Catania 8	Foundry*
Adv PMOS / VIP / MDMESH	Catania 8	Singapore 8	Foundry*
MEMS	Agrate 8	Catania 8	No

Front-End Manufacturing-Internal Fabs Value: Responsiveness, Differentiation, Efficiency

22

- Fast Time to Volume, to catch new business opportunities:
 - i.e. MEMS Gyroscope ramp-up within our 8" Fab



- Timely internal ramp-up of Crolles 12" ramp-up for Digital, Analog CMOS and Microcontroller (embedded Flash).
- Low cost & timely 8" conversion of the Singapore fab for discretes and mature BCD

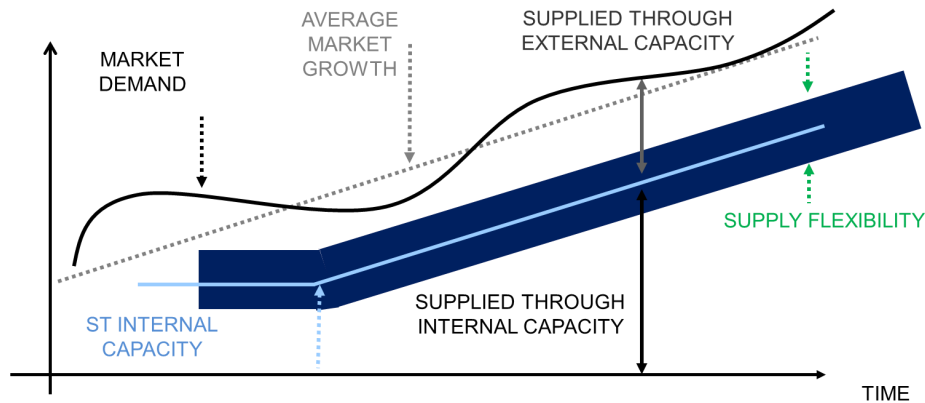
Packaging & Test Manufacturing: Flexibility/Efficiency

23

- Re-profile and balance some internal capacity
- Outsource proprietary packages growing volumes
- Complete Dual Source qualifications Internal vs. OSAT (subcontractors)
- Accelerate gold to copper wire conversion toward World Wide leadership
- Speed-up conversion to high density lead-frames
- Packaging & Test Manufacturing Hub for economy of scale, to call for alliance is a possible option we are working on to accelerate

Packaging & Test Manufacturing: Outsourcing Map

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Technology (Adv Logic) / Source	First: Time to Market	Second	Alternative
BGA - FC POP	OSAT*	Muar	Shenzhen
BGA - FC singulated	OSAT*	Malta	No
WLCSP	OSAT*	OSAT**	No

Technology (Others) / Source	First : Time to Market	Second	Alternative
BGA/ BGA-FC	Muar	Shenzhen	OSAT
MEMS	Malta	Calamba	No
Power Automotive	Muar	Shenzhen/ Bouskoura	Calamba
Power Discrete	Longgang	Shenzhen/ Bouskoura	OSAT**
QFN	Calamba	OSAT*	OSAT**
Imaging	Shenzhen	No	No
QFP small/Large	Muar/Malta	OSAT*	OSAT**
SOIC	Bouskoura	Shenzhen	OSAT*
Leadframe misc	OSAT*	OSAT**	No

Manufacturing and Technology R&D: 2012 Capital Spending

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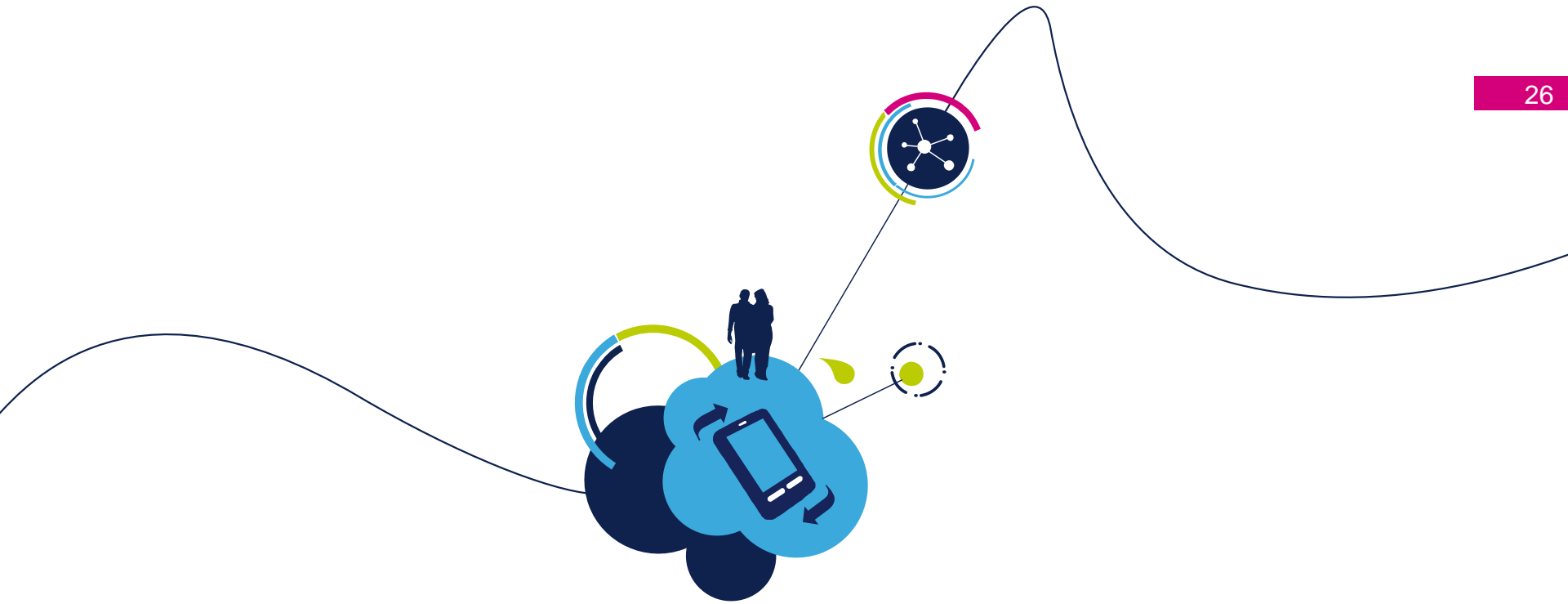
- Front-end manufacturing / R&D
 - 20 nm FDSOI capability
 - Crolles 300 mm 40 nm mix capacity increase
 - Imaging sensor BSI capability
 - Manufacturing and Engineering System
- Back-end manufacturing
 - Capacity increase and mix evolution at Asian plants
 - MEMS capacity increase
 - Manufacturing & Engineering System
 - Copper wire conversion
- Others
 - Testing, IT, quality & safety

2012 Capital Expenditures



Investments focused on:

- Strategic growth businesses and key product ramps
- Proprietary manufacturing



5. Conclusion