Manufacturing and Technology R&D

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Executive Vice President
Chief Manufacturing and Technology Officer
1. Introduction
Complete Products, IPs, & Technologies Portfolio

Power management, MEMS sensors, Analog, MCUs / ASICS, Automotive, Imaging, Smartphones and tablets, TV & digital set-top box

Power & Discrete, MEMS, BCD, eNVM, Analog Mixed Signal/RF, Advanced CMOS

Leadframe package leaded / leadless, MEMS, Leadframe package leaded / leadless, Laminated substrate package wired, Laminated substrate package flipchip, WLSP & 3D Integration
Technology R&D Model

Technology Competitive Advantage

« More than Moore »: Diversification
- Analog / RF
- Passives
- HV Power
- Sensors, Actuators
- Biochips

SiP
- SoC and SiP mix for Higher Value Systems
- Interacting with people & environment
- Non-digital content
- System-in-package

SoC
- Information processing
- Digital Content
- System-on-chip

CMOS Technology Alliances

Pre T0 Alliance: Advanced R&D
- 14nm Finfet
- FDSOI

ISDA: Bulk/low-power (LP) technology
- 32/28nm
- 20nm

* Renesas is only part of the Pre T0 Alliance

VLSI PLATFORM
Technology R&D Model

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An Unwavering Commitment to R&D

- 7 main technology R&D centers
- 39 design centers – 20,000 patents
- 12,000 people in technology, design, product and system R&D

VLSI PLATFORM

Beyond CMOS: Quantum Computing, Molecular Electronics, Spintronics
Flexible and independent manufacturing
2. Technology R&D
Multimedia convergence is about…

- Cloud (link between Network and Consumer equipment)
- Home servers and Gateways
- Connected Clients (OTT, Android, HTML5)
- Multi-screen, multi-application

Cloud

- Smart TV 3D
- Server and Gateways
- STB
- Tablet
- Smartphone

Performance
- Design simplicity
- Cost of ownership
- Power leakage
- Area scaling
Multimedia Convergence: 28nm Bulk Weaknesses

**Peak performance vs. energy efficiency**

- Energy efficiency (DMIPS/mW) vs. Vdd
- Gain by traditional scaling vs. Vdd
- Peak performance vs. Vdd

**Transistor performance improvement**

- Relative % Improvement for different technology nodes:
  - 180 nm
  - 130 nm
  - 90 nm
  - 65 nm
  - 45 nm
  - 32 nm

- Gain by traditional scaling and innovation for each node.
Multimedia Convergence: Fully Depleted Devices Enabling sub-20nm Technologies

• Main candidates after bulk are fully depleted devices
  • For improved electrostatic control and device scalability
Multimedia Convergence: 28nm FDSOI Better Energy Efficiency

Comparison of Energy Efficiency (DMIPS/mW) and Peak Performance (DMIPS) at different Vdd levels:

- **Energy Efficiency**: The FDSOI technology offers up to 3x better energy efficiency compared to bulk technology.
  - At a Vdd of 0.5, FDSOI achieves 4.7x better efficiency compared to bulk.
  - At a Vdd of 0.5, FDSOI achieves 6x better efficiency compared to bulk.

- **Peak Performance**: FDSOI also provides better peak performance compared to bulk technology.
  - At a Vdd of 1.1, FDSOI has a peak performance that is 1.3x better than bulk.

The diagram illustrates the comparative performance and efficiency across different voltage levels, highlighting the advantages of FDSOI technology in terms of energy efficiency and peak performance.
Multimedia Convergence: Value Proposition

Planar Technology – 2D

• High Logic/Memory Integration
• More complexity added to the process
• Available for Design: Q4 2012
• Enable New High Performance Product

28nm LP High-K/Metal gate

28nm Boost FDSOI/UTBOX

• Available for Design: Now!
• Superior Power Performance
• Faster Design
• Enable Product Cost / Power Reduction

20nm LPM Strained-Silicon

20nm Boost FDSOI/UTBOX

14nm Bulk-Trigate

• Available for Design: Now!
• Superior Power Performance
• Faster Design
• Enable Product Cost / Power Reduction

2012
2013
2014
2015
2016

28nm Boost FDSOI/UTBOX

• +30%
• +35%
• +20%
• +35%

20nm LPM Strained-Silicon
Other VLSI Key Differentiation Initiatives

- Embedded Flash PCM for future shrink nodes
- Ultra Fast and Low Power Microcontrollers
- Imaging sensor with BSI on bulk
Smart Power: The Ideal Technology

**POWER DEVICES**
- Figures of merit:
  - Rsp = RonxA
  - Gate charge (Qg) – Fsw up to 5 MHz
  - Safe operating area
- Trends:
  - Integration density saturating with LITHO scaling
  - Device architecture and drain engineering
  - Thick copper metallization for high current

**ISOLATION**
- Thick Cu metallization & bonding over active areas
- Junction isolation
- DTI (Deep Trench Isolation)
- SOI

**LOGIC**:
- from 100 K gates up to 500 K gates
- e-Memories

**ST ROADMAP**
- BCD8sP best in class for Power devices integration capabilities
- Customized solutions by application → Low Maks Count
- BCD9s (110 nm) ready for prototype in Q113 and BCD10 (90 nm) process architectures in definition phase
Full Copper Metallization

Power areas comparison vs. BCD6s-DCu

- Power Areas from Rdson (BCD6s-Dcu=1)
- Power Areas from energy pulsing

BCD6s-DCu: 1.0
BCD8sAuto: 0.7
BCD9s: 0.5

- 33%
- 30%
POWER: Top Priority Technology Platforms

- IGBT
- SiC
- GaN
- MD6
- OFT
SENSE: Technology Coverage

**SENSORS**
- Accelerometers
- Gyroscopes
- Compasses
- iNEMO™
- Pressure
- MicroPhone

**ACTUATORS**
- Thermal
- Piezoelectric
- Electrostatic
Packaging Technology R&D

**Sense**
MEMS and microphones (LGAs), Optical modules and Imagers towards BSI

**Power & BCD**
High dissipation, miniaturized packages (PSSO, QFNs)

**Multimedia Convergence with advanced CMOS**
Integration and miniaturization based on BGAs. Towards Flip Chip & WLP
3. Manufacturing
Front-End Manufacturing: Flexibility/Efficiency

Manufacturing flexibility across market cycle

- Minimize unused capacity in the downturns and lean investment to support upsides:
  - Model deployment by technology cluster better balancing internal vs. external with new major initiatives:
    - Start new generation of BCD (Smart Power) outsourcing
    - Start CMOS 28/20 nm FDSOI outsourcing
    - Start advanced CMOS Imaging Sensor with BSI

- Guarantee in-out flexible sourcing at product level

- Make fixed cost variable wherever possible
### Technology / Source

<table>
<thead>
<tr>
<th>Technology / Source</th>
<th>First: Time to Market</th>
<th>Second</th>
<th>Alternative</th>
</tr>
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<tbody>
<tr>
<td>CMOS 45LP</td>
<td>Crolles 300</td>
<td>Foundry*</td>
<td>No</td>
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<tr>
<td>CMOS 40LP</td>
<td>Crolles 300</td>
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<td>Crolles 300</td>
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<tr>
<td>CMOS 28LP</td>
<td>Foundry*</td>
<td>Crolles 300</td>
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<tr>
<td>CMOS 28 FDSOI</td>
<td>Crolles 300</td>
<td>Foundry*</td>
<td>No</td>
</tr>
<tr>
<td>HCMOS9A</td>
<td>Crolles 200 / 300</td>
<td>Rousset 8</td>
<td>Foundry*</td>
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<td>CMOS65 / 55RF</td>
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<td>CMOS Imaging Sensor</td>
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<td>CMOS55 eFlash</td>
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</tr>
<tr>
<td>CMOS M10 / F10 eFlash / eEEPROM</td>
<td>Rousset 8</td>
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<td>BCD8</td>
<td>Agrate 8</td>
<td>Catania 8</td>
<td>Foundry*</td>
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<tr>
<td>Adv PMOS / VIP / MDMESH</td>
<td>Catania 8</td>
<td>Singapore 8</td>
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<tr>
<td>MEMS</td>
<td>Agrate 8</td>
<td>Catania 8</td>
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</tr>
</tbody>
</table>

* One out of multi-foundry sources
** Another one of multi-foundry sources
Front-End Manufacturing-Internal Fabs Value: Responsiveness, Differentiation, Efficiency

• Fast Time to Volume, to catch new business opportunities:
  • i.e. MEMS Gyroscope ramp-up within our 8” Fab

• Timely internal ramp-up of Crolles 12” ramp-up for Digital, Analog CMOS and Microcontroller (embedded Flash).

• Low cost & timely 8” conversion of the Singapore fab for discretes and mature BCD
Packaging & Test Manufacturing: Flexibility/Efficiency

• Re-profile and balance some internal capacity

• Outsource proprietary packages growing volumes

• Complete Dual Source qualifications Internal vs. OSAT (subcontractors)

• Accelerate gold to copper wire conversion toward World Wide leadership

• Speed-up conversion to high density lead-frames

• Packaging & Test Manufacturing Hub for economy of scale, to call for alliance is a possible option we are working on to accelerate
Packaging & Test Manufacturing: Outsourcing Map

<table>
<thead>
<tr>
<th>Technology (Adv Logic) / Source</th>
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<th>Second</th>
<th>Alternative</th>
</tr>
</thead>
<tbody>
<tr>
<td>BGA - FC POP</td>
<td>OSAT*</td>
<td>Muar</td>
<td>Shenzhen</td>
</tr>
<tr>
<td>BGA - FC singulated</td>
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<td>Malta</td>
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<tr>
<td>WLCSP</td>
<td>OSAT*</td>
<td>OSAT**</td>
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<table>
<thead>
<tr>
<th>Technology (Others) / Source</th>
<th>First: Time to Market</th>
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<th>Alternative</th>
</tr>
</thead>
<tbody>
<tr>
<td>BGA/ BGA-FC</td>
<td>Muar</td>
<td>Shenzhen/ Bouskoura</td>
<td>OSAT</td>
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<tr>
<td>MEMS</td>
<td>Malta</td>
<td>Calamba</td>
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<tr>
<td>Power Automotive</td>
<td>Muar</td>
<td>Shenzhen/ Bouskoura</td>
<td>Calamba</td>
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<tr>
<td>Power Discrete</td>
<td>Longgang</td>
<td>Shenzhen/ Bouskoura</td>
<td>OSAT**</td>
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<tr>
<td>QFN</td>
<td>Calamba</td>
<td>OSAT*</td>
<td>OSAT**</td>
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<td>Imaging</td>
<td>Shenzhen</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>QFP small/Large</td>
<td>Muar/Malta</td>
<td>OSAT*</td>
<td>OSAT**</td>
</tr>
<tr>
<td>SOIC</td>
<td>Bouskoura</td>
<td>Shenzhen</td>
<td>OSAT*</td>
</tr>
<tr>
<td>Leadframe misc</td>
<td>OSAT*</td>
<td>OSAT**</td>
<td>No</td>
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Manufacturing and Technology R&D: 2012 Capital Spending

• Front-end manufacturing / R&D
  • 20 nm FDSOI capability
  • Crolles 300 mm 40 nm mix capacity increase
  • Imaging sensor BSI capability
  • Manufacturing and Engineering System

• Back-end manufacturing
  • Capacity increase and mix evolution at Asian plants
  • MEMS capacity increase
  • Manufacturing & Engineering System
  • Copper wire conversion

• Others
  • Testing, IT, quality & safety

2012 Capital Expenditures

Plan: $0.7B to $0.8B

Investments focused on:
• Strategic growth businesses and key product ramps
• Proprietary manufacturing
5. Conclusion