proceedings docket nr.8237/00   Justice Galletti

RAMBUS   Applicant

against

MICRON TECHNOLOGY ITALIA ad others   Defendants

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COURT EXPERTS REPORT

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1.1) PREAMBLE

The undersigned Dr. Ing. Paolo Stucovitz, member nr.328 of the Roll of the Intellectual Property Attorneys and member of the Roll of the Technical Experts of the District Court of Milan and Dr. Ing. Giorgio Crovini, member nr.857B of the Roll of the Intellectual Property Attorneys, were appointed as technical experts in the present proceedings and commenced the technical examinations on December 5th, 2000, as per the attached transcript (Att.1).

In the course of the technical examinations three briefs were respectively filed by the applicant and the defendants, the original of which are attached as 1Ri / 2Ri / 3Ri, 1Re / 2Re / 3Re. The defendants also filed a letter (attached) commenting the applicant's third technical brief to which the applicant replied with a letter dated April 26th, 2001 (attached).

In order to enable the technical examinations to proceed in a balanced way and with the consent of the parties, we applied for a postponement of the deadline for the filing of the Court Experts Report. A final deadline was established on May 2nd, 2001.

1.2) Queries

The following queries were submitted to the Court Technical Experts:

1)   may the experts duly assess the extrinsic and intrinsic novelty of the

invention at the date of the precedence claimed by the depositor, after having examined the appeal lodged on 26.12.2000 attached to the documents, in the light of the prior art submitted by the defendants and the available knowledge, having acquired the documents and acts deemed necessary regarding European patent proceedings, in reference to which the applicant is the title holder of the European patent, in reference to the claims made and in the light of the descriptions and drawings attached;

2) may the experts also state whether the invention is described in the patent in a sufficiently clear and complete manner, to permit an expert person to implement the said invention;

3) in conclusion, may the experts also state whether the object of the patent has been extended during the proceedings beyond the framework of the initial document;

4) in the event of a positive response to queries A and B and a negative response to query C, after the necessary technical examinations and investigations, also by availing of the support of specialized third parties, natural persons, as well as public or private structures, may the experts verify whether the devices subject of the application and currently subject to seizure may be deemed counterfeit of the exclusive right as indicated above, in the sense that the aforesaid provide solutions to technical problems resolved by the said exclusive privilege which are at least "equivalent" in functional terms, according to the knowledge of people skilled in the art.

1.3) Preliminary comments on the queries

We believe that, in order to facilitate the understanding of the present subject and to give a logical sequence our work, it is convenient to address the queries in accordance with the following matters:

- sufficient description;

- extension of the patent scope beyond the content of the original application;

- patent validity;

- infringement.

For the sake of convenience, we will use the following terminology:

novelty: extrinsic novelty;

inventive step: extrinsic inventive step.

2) PATENT IN SUIT NR. 0 525 068

The patent in suit was filed under the PCT Convention on April 16th, 1991 with application nr.PCT/US91/02590 entitled "INTEGRATED CIRCUIT I/O USING A HIGH PERFORMANCE BUS INTERFACE", claiming US priority nr.510898 on April 18th, 1990.

With the regional validation as European patent, which followed the filing of application nr.91908374, the patent was granted on April 19th, 2000 under nr. EP 0 525 068 with the title "SEMICONDUCTOR MEMORY DEVICE".

As illustrated in the front page of publication B1 of the patent, as a result of the several independent and non unitary claims contained in the original PCT application, the same European patent application generated three divisional applications (99118308.4 / 00101832.4 / 001000018.1).

2.1) The patent technical sector

In order to outline the detailed subject of the patent in suit, we believe it useful to briefly mention the general technical sector to which the patent refers.

It is well known that in several digital electronic appliances, such as computers, control devices (= CPU = MASTER = CONTROLLER) are used in order to process the data stored in the permanent / temporary memory devices (DRAM = SLAVE) to which the MASTER is connected by means of an intermediate connecting element having the function of carrying the information exchanged between the MASTER device and the SLAVE device.

A DRAM (Dynamic Random Access Memory) is a type of the above memory devices.

In more detail, each DRAM is constituted of proper circuits, integrated on a chip,

able to store a high number of single digital elements called bits that, properly combined with each other, form words representing information useful for data processing.

Each information bit is stored in a different physical location called DRAM memory cell and each memory cell is located at the intersection between a row and a column of the matrix configuration which is typical to a memory element.

In order for such information to be stored (=WRITE) / taken (= READ) into / from a memory device three information elements are needed:

- control information;

- address information;

- data information.

The control information tells the DRAM which operation has to be performed: write new data into the memory or read data already stored in the memory.

The address information provides the exact location in the memory where the operation read / write has to be performed.

The data information constitutes the actual information to be written, in order to be stored, or read, being useful to the CPU to executed a given processing.

All the above mentioned read / write operations and dialogue operations between the CPU and each memory element are carried out using the said connecting element on which all the information travel from/to the CPU and the memories.

Two fundamental methods of connections between the memories and the CPU have been provided for:

- point-to-point connection;

- bus connection.

The first consists in providing for a line for each connection between the memory device and the CPU.

This means that the signal gets to an only device directly enabling it, without

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needing any procedure in order to recognize the device to which the information is sent.

This system has the advantage of directly enabling the device so that less control information as well as less processing circuits are needed. However, it produces an unacceptable increase in the number of physical connections necessary to the functioning of the whole system.

To the contrary, a bus connection provides for a group of conductors to which the devices are connected in parallel, carrying data, address and control information (normally represented by words).

The data sent to the bus get multiplexed/de-multiplexed and the serial data output/input into/from the device are transformed into parallel data in order to have access to the bus and vice-versa.

Due to the higher and higher speed in which control devices are able to process data, in the processing systems the time element is more and more crucial, i.e. the capability of a single device to perform the required operation (read/write) in a prefixed time substantially representing the time needed by the device to take/put from/into the bus the provided/required data.

When a processor (=CPU) attempts to read a memory location in a memory device, the request is usually very urgent, in order not to stall the CPU. The most sophisticated CPUs are in fact able to respond to a number of requests at a time, but, due to their processing speed (much higher than the data exchange speed) sooner or later they will stop processing if the memory devices with which they exchange data are not quick enough.

The speed of a memory is often also indicated in latency terms, i.e. the delay transpiring between the time in which the processor requests an information and the time in which the latter is made available by the memory for use by the processor.

Within the variable "time", the concept of synchronous/asynchronous has to be considered, i.e. the fact that the operation to transfer data from/onto the BUS are carried out:

in a synchronous manner = the exchange of information from/to the bus is carried out synchronously with respect to a single clock signal;

in an asynchronous manner = the exchange of information from/to the bus is not carried out in accordance with a single clock signal (in particular the one of the bus) but in an independent way.

2.3) Definitions

Before examining the solution proposed by the claims, also based on the above paragraphs, we believe it useful to outline a few definitions fundamental to the technical discussion and the present report:

BUS = a group of conductors, positioned between a control device (CPU) and a memory device (DRAM) or similar, carrying data, address and control information, thus capable of enabling the exchange of data usually in word form;

ASYNCHRONOUS BUS = BUS in which all data transfers are not synchronized in even intervals with respect to a relevant clocking signal. It is then necessary for the device receiving the information to send back a signal confirming receipt, thus causing an increase in time wasting in the use of the bus.

SYNCHRONOUS BUS = BUS in which all data transfers are carried out synchronously with respect to a single clock signal. The synchronous BUS usually enables a better

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capacity of information since it is based on the assumption that, thanks to clocking, the device which had to receive the information has in fact received it, without the need of any confirmation signal.

MULTIPLEXED BUS = BUS in which information distributed according to time criteria are carried on the same conductor (=in a time distribution).

CLOCK = Temporizing impulse providing the synchronization element for the various functional phases of the various devices.

DRAM = DYNAMIC RAM = memory device which periodically restores the load level of the condenser representing the physical element in which the memories are realized.

LATENCY TIME / ACCESS TIME = The time (in clock cycles) needed by a memory to make information available on the bus.

CYCLE TIME = Sum of the access time and the time needed to send a signal confirming receipt in case of an asynchronous bus.

3) ON QUERY 1: SUFFICIENCE OF DESCRIPTION

3.1) The technical problem

As illustrated in the text of the patent (page 3) the technical problem at the basis of the patent is:

"to provide a semiconductor memory device to support high speed access to large blocks of data by an external user of the (same - added by the present drafter) data, such as a microprocessor, in an efficient and cost effective manner.

Another object of this invention is to provide a semiconductor memory

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device, suitable for use with the bus architecture described in the description".

3.2 Solution of the problem - claims.

With regard to the above mentioned technical problem the solution is, as usual, indicated in the only independent patent claim reading as follows:

1) A semiconductor memory device having at least one memory array (1) which includes a plurality of memory cells, the memory device comprising

+ clock receiver circuitry (101, 111)

  for receiving an external clock signal (53, 54)having a fixed frequency

+ a programmable access-time register

  for storing a value which is representative of a number of clock cycles of the external clock signal (53, 54)to transpire after which (<u>which have to transpire before - added by the present drafter</u>) the memory device responds to a read request and

+ a plurality of output drivers (76)

  for outputting data onto an external bus (18, 65) in response to a read request,

  wherein the output drivers (76) output data on the external bus (18, 65) after the number of clock cycles (<u>stored in the register - added by the present drafter)</u> of the external clock transpire

  and synchronously with respect to the external clock signal (53, 54).

In the subsequent claims preferred implementations are described, that will not be addressed for the time being.

3.3) Evidence in description and drawings.

By analyzing the description and the drawings on an exemplifying implementation, we will attempt to provide a complete explanation of the meaning of the above mentioned claim.

Given the fact that, as mentioned above, the original application used to include descriptive parts relating to a number of dependant inventions which gave origin to a number of divisional applications, we believe it useful to consider and analyze in detail only the parts of the patent text being directly connected with the content of the independent claim, omitting to consider any other part.

Let us go through claim 1:

+) A semiconductor memory device having at least one memory array (1) which includes a plurality of memory cells.

Page 12 reads ([0025] English version):

"all modern DRAM, SRAM or ROM designs have internal architecture (matrix type - added by the present drafter) with rows (words) and column (bit) lines to efficiently tile a 2-D area . Referring to fig.1

- Fig.1 -

one bit of data is stored at the intersection of each word line 5 and bit line 6.

When a particular word line is enabled, all of the corresponding data bits are transferred onto the bit lines.

This data, about 4,000 bits at a time in a 4 Mbit DRAM, is then loaded into column sense amplifiers 3 and held for use by the I/O circuits".

+) clock receiver circuitry (101, 111)

for receiving an external clock signal (53, 54)having a fixed frequency
SYNCHRONIZATION

"Clocking a high speed bus accurately without introducing error due to propagation delays can be implemented by having each device monitor two bus clock signals and then derive internally a device clock, the true system clock. The bus clock information can be sent on one or two lines to provide a mechanism for each bused device to generate an internal device clock with zero skew relative to all the other device clocks.

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- Fig.8a -

- Fig.8b -

Figure 8b illustrates how each device 51;52 receives each of the two bus clock signals at a different time (because of propagation delays along the wires), with constant midpoint in time between the two bus clocks along the bus.

As each device 51;52, the rising edge 55 of clock1 53 is followed by the rising edge 56 of clock2 54.

Devices which are closer to the clock generator have a greater separation between Clock1 and Clock2 relative to devices farther from the generator because of the longer time required for each clock pulse to traverse the bus and return along line 54 but the midpoint in time 59;60 between corresponding rising or falling edges is fixed because, for any given device, the length of each clock line between the far end of that device is equal.

Each device must sample the two bus clocks and generate its own internal device clock at the midpoint of the two in order to avoid synchronization differences caused by the accumulation of the clock signal propagation delays.

A block diagram of the internal device clock generating circuit is shown in figure 12.

A DC amplifier 102 is used to convert the small-swing bus clock into a full-swing CMOS signal.

- Fig.12 -

This signal is then fed into a variable delay line 103. The output of delay line 103 feeds three additional delay lines 104; 105; 106.

The outputs 107, 108 of the delay lines 104 and 105 drive clocked input receivers 101 and 111 connected to early and late inputs 100 and 110… (omissis).

Variable delay lines 103 and 105 are adjusted via feedback lines 116, 115 so that input receivers 101 and 111 sample the bus clock just as they transition (omissis).

Since the outputs 107 and 108 are synchronized with the two bus clocks and the output 73 of the last delay line 106 is midway between outputs 107 and 108, output 73 provides an internal device clock midway between the bus clocks.

The falling edge 124 of internal device clock 73 precedes the time of actual input sampling 125 by one sampler delay.

Note that (omissis) outputs 107 and 108 are adjusted so the bus clocks are sampled by input receivers 101 and 111 just as the bus blocks transition".

+)   a programmable access-time register

for storing a value which is representative of a number of clock cycles of the external clock signal (53, 54)to transpire after which (which have to transpire before - added by the present drafter) the memory device responds to a read request;

Each semiconductor device contains a set of internal registers …"

"the semiconductor devices connected to the bus contain registers which specifies the memory addresses contained within that device and access time registers which store a set of one or more delay lines at which the device can or should be available to send or receive data.

Most of these registers can be modified and preferably are set as part of an initialization sequence that occurs when the system is powered up or reset."

"each slave may have one or several access-time registers (…) In a preferred embodiment, one access-time register in each slave is permanently or semi-permanently programmed with a fixed value to facilitate certain control functions."

+) a plurality of output drivers (76)

for outputting data onto an external bus (18, 65) in response to a read request,

wherein the output drivers (76) output data on the external bus (18,

65) after the number of clock cycles (stored in the register - added by the present drafter) of the external clock transpire

and synchronously with respect to the external clock signal (53, 54).

ELECTRICAL INTERFACE - INOUT/OUTPUT CIRCUITRY

A block diagram of the preferred input/output circuit for address/data/control lines is shown in figure 10.

- Fig.10 -

It consists of:

- a set of input receivers 71, 72 and output driver 76 connected to input/output line 69 and pad 75 and

- circuitry to use the internal clock 73 and internal clock complement 74 to drive the input interface.

The clocked input receivers take advantage of the synchronous nature of the bus (omissis).

By thus de-multiplexing the input 69 at the pin, each clocked amplifier is given a full 2ns cycle to amplify the bus low-voltage-swing signal into a full value CMOS logic signal (omissis).

The output drivers are quite simple, and consist of a simple NMOS pulldown transistor 76…(omissis).

This output driver which can be operated at 500MHz, can in turn be controlled by a suitable multiplexer with two or more (preferably four) inputs connected to other internal chip circuitry, all of which can be designed according to well known prior art."

As a consequence we believe that the patent is sufficiently described for a person skilled in the art to implement it. We also believe that the subject of the independent patent claim finds its evidence and explanation in the patent text.

4) INTERPRETATION OF THE CLAIM AND EFFECT OF THE INVENTION

Claim 1 of the patent in suit, supported by the description (the quotes in square brackets indicate the corresponding paragraph in the English version of the patent in suit), refers to a "semiconductor memory device" which in a preferred embodiment, described as an example, appears to be an evolution of a DRAM memory, known in prior art [0017], to obtain a memory quick, synchronous, ("a receiver circuitry for receiving an external clock signal") capable of determining a synchronous high speed transfer of data blocks [0014] between a memory and a CPU by means of a connection bus.

The detailed description [0023] specifies that the memory device is for use with a high speed, synchronous and highly multiplexed bus, and, in this respect, it is clarified that multiplexed means with a time distribution [0081].

The bus carries substantially all address, data and control information required by the devices to communicate with the other devices on the bus.

The time correlation between the read request, the number of cycles of the external clock and the synchronous output of data onto the external bus - interpreted in light of the object of the patent which is to enable the use of the bus during the cycles transpiring between the request and the data output - renders it necessary to manage the data according to a rigorous timing with respect to controls, data and addresses.

It is also stated that in many systems used with the present invention the bus carries each signal of the system.

In particular, the memory described has to be modified in order receive and output data:

-) in "normal mode" (= pre-charge of row sense amps) [0049]

-) in synchronous "page mode" (=cache) by keeping available a frequently used

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information and by synchronously [0049] and burst outputting, also at the peak bus frequency [0019].

This requires that the access circuitry of the DRAM be modified. In more detail, among the modifications of the above said semiconductor devices, the use of register is included, comprising:

-) the memory addresses contained in the device and

-) an access-times register in which it is possible to store a plurality of configurable numbers, each of which is representative of a prefixed delay after which the device can or should be available to send or receive data [0028].

Consequently, a request packet coming from the CPU and the corresponding bus access response by the memory, are separated by a time interval (delay), represented by a number of clock cycles. Such delay is chosen according to the type of the request among the values available within the register. This enables the CPU to use the BUS during the programmed number of clock cycles to send other requests to the same or other slaves.

Ion this way, multiples and independent accesses to the slave are permitted, thus enabling the maximum use of the bus top transfer small data blocks [0030-0031].

In the patent it is not indicated whether the number of clock signal cycles stored in the register is a non integer number, an integer number or a multiple of a clock signal period. However, a fraction number smaller than 1 does not seem to be coherent with the object of prolonging the memory latency time in order to enable a master to exploit the intervening clock cycles.

These paragraphs then show that the goal of the claimed solution is substantially to enable the maximum possible speed in connection to the read of small data blocks together with the possibility to free the bus in the event of a long latency period.

In particular, in the "page mode", the above is facilitated by the use of an access

register. The latter, in fact, makes it possible to take into account the latency time penalty occurring when the request refers to data which are not already contained in the read amplifiers [0047 / 0049] and the memory is obliged to unload the pre-data already available, to switch to the "normal mode" and to obtain the new data in order to make them available on the bus.

Therefore, one of the main effects of the use of an access time register seems to be the implementation of a more efficient synchronous cache memory (=memory that always keeps available a given information which statistically is frequently required) [0050].

The above without the need of any external auxiliary device.

By summarizing and interpreting the features of the memory device specified in the independent claim, we find that:

A semiconductor memory device having at least one memory array (1) which includes a plurality of memory cells.	a memory device
Clock receiver circuitry (101, 111) for receiving an external clock signal (53, 54)having a fixed frequency	The memory device is synchronous since it receives a clock signal from the outside.
+) a programmable access-time register for storing a value which	A register storing access time values in a modifiable manner
is representative of a number of clock cycles of the external clock signal (53,	A time delay which is a number of clock cycles

54)	
to transpire after which the memory device responds to a read request;	before the output of data, a stored number of clock cycles from the synchronous arrival of the read request has to transpire
a plurality of output drivers (76)	Any driver capable of putting data onto the bus according to a clock signal
for outputting data onto an external bus (18, 65) in response to a read request,	the external bus is at least synchronous
Wherein the output drivers (76) output data on the external bus (18, 65) after the number of clock cycles of the external clock transpire and synchronously with respect to the external clock signal (53, 54).	The drivers make the data available on the bus after the stored number of cycles of the external clock transpiring from the clock signal in which the request is registered.

5) ON THE SECOND QUERY: EXTENSION OF THE PATENT SCOPE

5.1) Preliminary comments

Once we have verified that the content of the current claim is supported by the text, we have to evaluate whether the European examination procedure led to an extension of the protection scope of the patent. To this end, it is necessary to compare the current claim 1, as granted, and the claim referred to in the patent application as filed, also considering the full text of the latter application, in order to decide whether new limitation elements have been introduced into the current

claim with respect to the original one.

5.2) Patent application PCT / US91 / 02590

As both parties have recognized, the current claim 1 derives from claim 103, reading:

103) A semiconductor device capable of use in a semiconductor bus architecture including a plurality of semiconductor devices connected in parallel to a bus wherein said bus includes a plurality of bus lines for carrying substantially all address, data and control information needed by said semiconductor device for communication with substantially every other semiconductor device connected to said bus, and has substantially fewer bus lines than the number of bits in a single address, said semiconductor device comprising

connection means adapted to connect said semiconductor device to said bus, and

at least one modifiable access-time register accessible to said bus through said connection means, whereby data may be transmitted to said register via said bus which establishes a predetermined amount of time that said semiconductor device thereafter must wait before using said bus in response to a request."

5.3) Differences between the two claims

Current claim 1 reads as follows:

A semiconductor memory device having at least one memory array (1) which includes a plurality of memory cells, the memory device comprising:

clock receiver circuitry (101, 111) for receiving an external clock signal (53, 54)having a fixed frequency;

a programmable access-time register for storing a value which is representative of a number of clock cycles of the external clock signal (53,54) to transpire after which the memory device responds to a read

request; a plurality of output drivers (76) for outputting data onto an external bus (18, 65) in response to a read request, wherein the output drivers (76) output data on the external bus (18, 65) after the number of clock cycles of the external clock transpire and synchronously with respect to the external clock signal (53, 54).

We note that the following paragraphs have been removed:

"capable of use in a semiconductor bus architecture including a plurality of semiconductor devices connected in parallel to a bus wherein said bus includes a plurality of bus lines for carrying substantially all address, data and control information needed by said semiconductor device for communication with substantially every other semiconductor device connected to said bus, and has substantially fewer bus lines than the number of bits in a single address"

"connection means adapted to connect said semiconductor device to said bus".

The above paragraphs refer to implementation details concerning the features of the bus to which the memory device has to be connected and the means used to enable the connection between the memory and the bus.

Said bus is described in the patent as follows:

BUS

The bus architecture used in combination with this invention comprises 11 signals: BusData; AddrValid; ClK1 and ClK2 (…) the bus lines for BusData signals form a byte-wide, multiplexed data/address/control bus.

AddrValid is used to indicate when the bus is holding a valid address request, and instructs a slave to decode the bus data as an address and, if the address is included on that slave, to handle the pending request.

The two clocks ClK1 and ClK2 together provide a synchronized, high

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speed clock for all the devices on the bus (…)

To facilitate the extremely high data rate of this external bus relative to the gate delays of the internal logic, the bus cycles are grouped into pairs of even/odd cycles.

Note that all devices connected to a bus should preferably use the same even/odd labeling of bus cycles and preferably should begin operations on even cycles.

This is enforced by the clocking scheme.

PROTOCOL AND BUS OPERATION

The bus uses a relatively simple synchronous spilt-transaction, block-oriented protocol for bus transactions.

One of the goals of the system is to keep the intelligence concentrated in the ,masters, thus keeping the slaves as simple as possible (since there are typically many more slaves than masters).

To reduce the complexity of the slaves, a slave should preferably respond to a request in a specified time, sufficient to allow the slave to begin or possibly complete a device-internal phase including any internal actions that must precede the subsequent bus access phase.

The time for this bus access phase is known to all devices on the bus, each master being responsible for making sure that the bus will be free when the bus access begins.

Thus the slaves never worry about arbitrating for the bus. This approach eliminates arbitration in single masters systems, and also makes the slave-bus interface simpler.

Also considering the interpretation of the patent provided for in the preceding paragraphs, we believe that the bus simply represents the connection element between master and slave, being the bus subject to the protocol rules of such

connection.

Consequently, the bus does not have to be considered as an intrinsic element of the semiconductor memory device, being rather an external element with which said device needs to be connected and with which it has to interact.

From a different point of view, we understand that once a new bus architecture has been established (hardware + software) it is necessary to provide for all the devices needing to be physically connected to the bus and needing to interact with the same, to be adapted to work correctly with the specific bus and, in the event that they are not already adapted, to be modified accordingly.

As far as memories are concerned, such modification (adaptation) consists, in the present case, in the programmable access-time register and the output driver which is synchronized with the bus clock in order to output data at a prefixed time and synchronously with respect to the bus.

From this point of view the claimed semiconductor memory device is, within the patent, independent from the bus element and what constitutes the connection element between the two (memory/bus) is the synchronization clock.

Here comes the solution of providing for a programmable access time register and a plurality of output drivers outputting data onto the bus after a programmed time, in synchronism with respect to the bus, in order to enable the most proper synchronous clocking for the slave response (on the bus) to the master request.

We then believe that the protection scope of the patent in suit **did not** result from an illegitimate broadening occurring during the European examination procedure. Such scope was simply redefined in relation to one of the several independent solutions which where comprised in the original application.

6) PRIOR ART

During the technical examinations several documents were filed regarding prior

art at the time of the priority claimed by the patent in suit.

Some of such documents were filed attached to an application for opposition against the granting of the patent. Some others were filed as attached to the first brief of the defendants.

We note that many documents were simply filed in order top demonstrate the lack of novelty of dependent claims according to a traditional approach for the opposition procedure before the EPO. However we think that such documents are redundant for the scope of the present report, which has to be submitted in the frame of urgent proceedings.

Consequently we will address and comment only the documents that we believe relevant for the scope of the present technical report., also considering that the patent in suit has already been granted following to EPO examinations.

The selection of the documents to be addressed was of course made among **all** the documents filed.

In a chronological order, the relevant documents are the following:

6.1.) JP S54 - 160587 (KAWAMASA)

This patent application was published on July 7th, 1981, thus constituting valid prior art both under Art.14 and Art.16 Law of Inventions.

The technical problem which this document proposes to resolve is employing different speed memories (page 2).

The documents generically leads to work synchronously with respect to the bus, performing the fetching, i.e. providing the required information after a given number of cycles (e.g. 5).

This way of working is defined as known and as presenting problems in synchronizing the clock signals between the memory and the CPU.

The proposed solution is to set a fixed value circuit (11) feeding a counter (7) which is selected for the operation by means of proper control signals.

The fixed value circuit 11 is external with respect to the memories. Furthermore, according to the solution of this document, the fixed value circuit is alternatively replaced in its function of setting the counter 7 by arithmetic-logic unit 10. On page 3 of the translation we note that the counter 7 is every time loaded with a correlated time, being the response time of the specific memory to which access is intended. Once such time has transpired, the data read on a control register of output 6 are made available.

The memory device has the function of confirming that the access time has actually transpired.

It is then a device managing memories working at different speeds and not different access times of the same memories.

6.2) US 4, 445, 204 (NISHIGUCHI)

The patent was published on April 24th, 1984, thus constituting valid prior art both under Art.14 and Art.16 Law of Inventions.

The Nishiguchi document describes a ROM memory interacting with a CPU.

The technical problem indicated in this document is the fact that a long access time to the memory obliges the CPU to stretch the duration of the read signal.

Nishiguchi resolves this problem by introducing for a READY SIGNAL GENRATOR 2 providing for a ready signal to the CPU with a delay fixed through a number of clock cycles. Such clock CL, which is the memory clock, is not indicated as synchronous with respect to the clock signal of the CPU. The CPU, in response to the ready signal, sends, according to a not indicated timing, an OC signal activating the drivers.

We then understand that the ROM memory is not synchronous and that it has no synchronous driver.

Furthermore, the programming of the delays is static and hardware type.

6.3) US 4,999,536 (GEMMA)

The patent was published on February 12th, 1085, thus constituting valid prior art both under Art.14 and Art.16 Law of Inventions.

This document describes the control apparatus of a memory, containing clocking information based on the performances of a memory and a processor.

Such control apparatus uses a Storage Controlling Unit device (SCU 19) external with respect to the memory, which produces specific problems (2:52-55). The problems are in fact cause by the fact the control apparatus is external.

It is also stated that the memory transmits signals to the processor only after having received a send signal by the SCU, thus determining a an asynchronous functioning.

Therefore, Gemma teaches to produce: a device which is not a memory, according to an asynchronous functioning, in order to resolve a technical problem which, although concerning the clocking of data exchange between a processor and memory devices, has nothing to do with the problem resolved by the patent in suit.

6.4) JP-58-186919 (HASEGAWA)

The patent application was published on May 8th, 1985, thus constituting valid prior art both under Art.14 and Art.16 Law of Inventions.

The technical problem which it proposes to resolve is to avoid the need to individually control the clocking of memories with different speeds.

The solution is conceptually very similar to the one in Kawamasa, even though it is different from with respect to the implementation. In Hasegawa, in fact, memory means 2 or 3 are available to store a binary value which is progressed in a shift register, determining different times depending on the binary value taken.

In this case the circuit is anyhow different. It is in fact located externally with respect to the memory, given to the fact that the device is of a type in which it is possible to have access to different types of memories, each with a specific and

optimized time.

6.5) THE 12G014 SYNCHRONOUS RAM in GIGABIT LOGIC 1988 GaAs IC DATA BOOK

The manual was published in August 1989, thus constituting valid prior art both under Art.14 and Art.16 Law of Inventions.

This document is the Gigabit manual for a static RAM memory in gallium arsenide.

The said memory receives the clock signal from outside (pages 2-3) and has three modes for outputting data: transparent mode, register mode and latch mode.

In the register mode (2-6) re access request is activated by a Write Enable signal, the access occurs during the corresponding clock signal cycle and the data output occurs on the following cycle.

In the latch mode, the access request is activated by a Write Enable signal, but, contrary to the above mode, the clock signal has a duty cycle modified cutting down the high logic level. Furthermore, the output latch circuits become transparent for the data (i.e. they do not retain the data) on the falling edge of the clock signal. The effect of such modifications is to provide the output data in a time shorter that half cycle of the clock signal.

The mode is set by way of the MODE PIN (2-4) tension. The register mode is programmed by connected the pin at tension VSS, the latch mode at tension VDD.

The conceptual differences in this document are represented by the fact that

- the delay clock cycles are 1 or less than half;

 - there is no register, but a pin which is programmed in hardware manner, i.e. dynamically;

- it is rather evident (2-5) that "register mode" means that the data are driven to the output by means of an output register, "latch mode" means that such output register is transparent and that the clocking is made on the falling edge of the

clock signal, while the "transparent mode" is not limited in any way in the output. The document does not describe any register to store the delay times.

The manual refers to a synchronous RAM of conventional type in which there is no dynamically programmable register to govern the response delay with respect to the read request in the meaning of the solution outlined in the patent in suit.

6.6) DE 37 42 487 KAWAI

the patent application was published on July 7, 1988, thus constituting valid prior art both under Art.14 and Art.16 Law of Inventions.

This document describes a variable delay circuit to delay the output of incoming data, to be used in communications systems for reasons of image synchronization. Such circuit seems to actually be a buffer delaying the output of data according to a signal of the external clock.

Nevertheless, given that it has the nature of a delaying element, it does not present anything similar to a read request. The first incoming data are the first to be output, after the programmed delay. It may be deemed as a sequence access memory (FIFO).

6.7) JP-62-71428 - YAMAGUCHI

The patent application was published on October 5th, 1988, thus constituting valid prior art both under Art.14 and Art.16 Law of Inventions.

The text of the patent shows that it refers to:

claim 1) A semiconductor memory device comprising

a serial-parallel circuit

> that receives a plurality of read data that is parallely output over a plurality of data lines constituting a memory array

> and provides a serial output in accordance with a clock signal from an external source

a timing control circuit

that controls the serial output operation of the aforesaid serial-parallel conversion circuit

characterized by

the timing for starting the aforesaid serial output being set at will

by specifying the number of cycles of the external clock signal required between activation by an activation signal from an external source and the start of the serial output operation.

Claim 2) The timing control circuit comprising

A counter circuit

That obtains the number of cycles from an external source in synchrony with the activation control signal and then performs a count-down operation in accordance with the aforementioned clock signal

A timing generation circuit

That creates an internal clock signal that is used for a serial output operation,

on detecting "0" at the output of the counter.

Claim 3) (omissis) and the aforementioned number of cycles being provided over a plurality of data input/output terminals for random access port use.

By reading the detailed description of an example embodiment we also understand that:

"The present invention relates to semiconductor memory devices and in particular to an art that is effective for example when used with a dual port memory … for image processing and possessing both a random input/output function and a serial input/output function."

Referring to the problem which the patent proposes to resolve

" …the timing for returning the level of the data transfer control signal DT/OE to high is determined by monitoring the output signal of the counter circuit in the memory control circuit".

Later in the document it is specified that "this results in an unstable serial data transfer and a distribution of the displayed images".

Therefore, this application describes a RAM memory device dual port type, i.e. provided with a first random access port and a second serial access port.

This kind of memory device is well known and is usually employed for the so called VRAM memories, i.e. the memories used to provide the video information being output by the graphical cards to the monitor. It is a memory device needing to be quick in order to provide data at the monitor refreshing rate, as illustrated by the document itself.

The reason of the dual port lies in the need to be able to contemporarily exchange information, on one side, with the CPU to perform graphical operations and, on the other side, with the monitor. This kind of memory is anyhow analogous to the DRAM other aspects.

This dual port memory contains a TC timing control circuit, which receives a SC signal of the external clock relating to the serial output and the output rate towards the monitor. Such TC circuit is governed by a CTR counter, which can be dynamically initialized with a value coming form the random access input, i.e. from the CPU, in order to perform a count-down in terms of cycles of an external clock signal, with the same rate of the SC external clock signal. The CTR counter is comprised in a control circuit of the horizontal location of the pixel on the cathode ray tube, therefore it is not comprised in the memory device. When the CTR counter reaches zero, the data is sent to onto the serial port of the memory synchronously with respect to the SC serial clock signal.

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Since the "read request" in Yamaguchi is formed by the RAS signal, which does not come from the external bus, but from other signal lines (the ones on the random access port) and given that the RAS signal is not synchronous with the SC clock signal, the counter function of Yamaguchi is only to re-synchronize the serial output, on a given number of cycles, in order to enable to annul possible port delays. On page 21, line 18 it is explicitly stated that the number of cycles is counted by the RAS signal.

Furthermore, in Yamaguchi the RAS signal does not indicate a read request to the memory, rather a data transfer request on another synchronous bus.

Notwithstanding language similarities between Yamaguchi and Rambus, i.e.

+) a memory device to which are associated

+) means to control the moment of the beginning of the memory response after that the memory has received an activation signal

+) such time being expressed in a number of cycles of an external clock;

+) such number of clock cycles being stored in a counter

+) the output of the signal being made synchronously with respect to the signal of an external clock

However we note that

-) the memory structure is different from Rambus memory structure in that it includes a random access port and a serial access port, comprising a parallel serial conversion circuit;

-) the output delay control and the output of the signal in synchronism relate to the serial part of the device;

-) the RAS signal determining the transfer request is asynchronous with respect to the serial clock signal which determines the synchronism of the transfer.

The dual port memory is conceived to function on two different buses: one multiplexed random and the other serial and not with a single synchronous bus.

6.8) US 4, 785, 428 (BAJWA)

The patent application was published on January 1st, 1989, thus constituting valid prior art both under Art.14 and Art.16 Law of Inventions.

Such document describes a (MCU)controller for DRAM memory.

The description of prior art shows that such controllers need to be adaptable to different kind of memories with different speeds and that the MCU known only enable a minimum adaptation level. It is indicated as desirable to have an MCU generating any timing scheme needed for the control signals of a RAM.

This is resolved by providing the MCU with its own program RAM, in which specific timing sequences for each DRAM type, of which employment is foreseen, can be stored and externally programmed.

The timing sequences comprise a sequence RPYNOW which can be programmed by the user to indicate to the MCU the clock cycle in which a packet of read data can be inserted.

The patent does not provide for any indication on:

a) the possibility to determine an incremental delay beginning from the read request;

b) the possibility to modify the delay in relation to the different kinds of access to the memory.

6.9) JP 62-185253 (KUMAGAI)

The patent application was published on January 31st, 1989, thus constituting valid prior art both under Art.14 and Art.16 Law of Inventions.

The document refers to a storage system comprising an external controller of the memory, the Storage Control Unit already mentioned, and a memory.

The technical problem is identified in the lack of clocking between the external controller and a memory.

The proposed solution first of all provides for a synchronization of the two elements using the same clock.

Furthermore, there is a controller of the RAM MCR comprising a counter 300 to generate a delayed CAS signal.

Even if the delayed CAS signal was equal to a read request signal, Kumagai would anyhow teach to delay the read request, not the output of data with respect to the read request.

The architecture described by Kumagai refers to a complex device including a part of memory and a part of memory control (MCR).

6.10) US 4, 853, 113 (SACCARDI)

The patent has been published on August 15th, 1999, thus constituting valid prior art both under Art.14 and Art.16 Law of Inventions.

The American patent named Saccardi describes a "pipelined" type parallel architecture processor. "Pipelined" generally means a processor performing a series of instructions in a consecutive manner., employing to such end a series of registers and arithmetic-logic units (according to scheme analogous to the one described in fig.1 of the document) that are then operated in a parallel manner.

In the document, such elements are connected by means of a "crossbar", i.e, in general, a commuter presenting a plurality of vertical paths and a plurality of horizontal paths, as well as proper electromagnetic means to interconnect them such as, for example, switch or equivalent in integrated electronics. According to figure 5, VTD (Variable Tick Delays) devices are positioned at input/output to/from the registers and to/from the arithmetic/logic units, in order to solve synchronization problems.

These VTDs are controlled by control bits C0 …C32 governing the number of delay registers that the VTD inserts on the data path, before having access to the memory device.

Therefore the patent shows that:

- the described device is a parallel processor and its memory devices are internal registers, not memories connected to the bus;

- the crossbar is not a bus, but a connection matrix;

- the VTD device is external with respect to the registers;

- For this reason the delay occurs before, and not after, the receipt of the access request by memory device. Figure 9 is clear in this respect; there never is direct access from the crossbar to the memory;

- it is not described on which lines the control bits C0…V31 are transmitted and they do not seem to drive on the same line used by the data to the VTD device.

Therefore, Saccardi does not seem to provide for any useful teaching to get to the solution proposed by the patent in suit and it seems to deal with very different problems.

7) NOVELTY

Keeping in mind that in evaluating novelty of the subject matter of patent nr. EP 0 525 068 after having compared, as is usual, the same patent with what is **individually** contained in each of the prior art documents, we conclude that none of the prior art documents filed describes in an identical and complete way a memory device such as the one claimed in the patent in suit, according to the interpretation outlined in section 4 of the present report.

In more detail, considering in particular the three documents on which the defendants based their nullity claim for lack of novelty, we outline the as follows.

a)   Yamaguchi describes a dual port device, with random and serial access, and the corresponding serial-parallel converter. The (RAS) signal determining the transfer request is asynchronous with respect to the serial clock signal determining the synchronism of the transfer. Therefore, the

read request is not synchronous with respect to the bus on which the output drivers output data. Furthermore, note that the claim of patent nr. EP 0 525 068 in suit requires for the programmable access time register to be comprised in the semiconductor memory, while in Yamaguchi at least the CTR counter, determining the timing together with the TC timer, is external with respect to the memory.

b) Gigabit Logic manual refers to a synchronous RAM of a conventional type in which there is no programmable access time register to govern the output of data with respect to the read request. The programming is carried out by way of the hardware wiring of a pin.

c) Saccardi describes a parallel processor with memory devices internal with respect to the processor itself. The so called "crossbar" is not an external bus, but rather a commutation device. The VTD devices cannot be deemed as programmable access time registers, but rather as programmable delay lines. Said access request devices are not comprised in the memory.

In the case of VTD positioned at the entrance, the delay occurs before, and not after, the receipt of the read request by the memory device

Consequently we believe that the subject matter of patent nr. 0 525 068 as limited by independent claim 1), as granted, **is provided with novelty characters** under Art.14 Law of Inventions with respect to the existing art at the date of priority of the patent in suit.

8) INVENTIVE STEP

Contrary to the evaluation of novelty, in assessing the inventive step of the subject matter of the patent in suit, it is possible to consider a combination of more than one document.

To this end, according to an evaluation method called "problem-solòution

approach", it is however necessary to identify which prior art document has to be considered as the most relevant prior art from which to start to identify the possibility to complete the information which such document does not provide for with the other information contained other documents. The latter have in turn to provide for such information in a direct manner and not following to a further interpretation. Otherwise there would be an inadmissible ex-post construction.

From this point of view, we believe that the document to be considered as the most logical starting point for a person skilled in the art is represented by the 12G014 of the Gigabit Logic manual of 1988, since we believe that, having to resolve a problem relating to synchronous memories, as person skilled in the art would have started by looking up the existing literature on such devices.

The Gigabit Logic describes a synchronous Ram memory, receiving a clock signal from the outside and having three data output modes: transparent mode, register mode and latch mode.

In register mode the access request is activated by a Write Enable signal, coming from the external bus. The access occurs during the corresponding clock signal cycle and the data output occurs in the following cycle.

As already outlined, the Gigabit memory does not provide for a programmable access time register.

Even admitting (thing which is not certain) that it was already clear that the solution of the problem had to be found in the use of a programmable access time register, we would still have to verify whether there were evident indications in the existing art leading to such a solution.

In this respect:

a)   Bajwa teaches a completely programmable device for managing different timing sequences proper to different memories. The device is external. Even admitting that Bajwa programmable RAM is equivalent to a simple

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access time register, in a possible integration of the Bajwa device in another synchronous memory, we have to note that the Bajwa document stresses the use of interconnected different memories, which seems to lead the person skilled in the art far from idea of integrating the device inside a synchronous memory, also, and especially, considering that the Bajwa device is destined, in the first place, to managing control signal timing sequences (RAS, CAS, WE…) on a memory bus. The integration of the Bajwa device within a DRAM would lead to annulling the main feature of the device itself, i.e. the output of the temporized sequences appropriate to each memory, by completely transforming the patent lesson.

The conclusion is analogous for the external controllers of Hasegawa and Kawamasa.

b)   Regarding the possibility to obtain the lesson of a programmable register internal with respect to the memory through Yamaguchi, we note that even though it is possible to find in such document a memory device with means to control the moment in which the memory response begins after the receipt of an activation signal, the access (transfer) request arrives in a manner totally asynchronous and on a completely different bus separated from the serial external bus on which the access times register operates. The separation between the random access port and the serial access port is the essence of a dual port memory, so that a person skilled in the art would have had to carry out an inventive effort in order to abstract from such a different context the Yamaguchi register and connect it to the single serial synchronous access port of Gigabit Logic. We believe that it would at least be a translating invention.

c)   Finally, Nishiguchi describes an asynchronous ROM memory containing a circuit to generate a ready signal, which can be delayed of a proper number

of cycles.

Besides the fact that the Nishiguchi memory requires a signal from the CPU, after the output of the ready signal, to output data, the element containing the delay information in Nishiguchi is constituted by an only switch register which is programmed in hardware manner at the time of the installation and cannot subsequently be modified. Therefore, in combination with Gigabit Logic, Nishiguchi would not lead to the invention.

As a support to the above analysis, we make two more considerations:

-) The arguments used by the defendants were not able to form a coherent reasoning explaining, starting from a document deemed as the most relevant one, how to take the missing part from another document in order to obtain in a direct and evident way the Rambus invention.

In this respect we underline that, in order to avoid an ex-post construction, it is not sufficient to highlight the generic possibility of combining more documents. It is rather necessary to identify an evident information which would feasibly lead enable to complete in an obvious manner a document and get to the solution of the later patent.

-) The defendants also have attached to their third brief the Rambus US patents regarding the memory in suit. As is illustrated in the front pages of these patents, during the exam preceding their granting, the patents -) Nishiguchi -) Yamaguchi -) Kawai were deemed relevant. Nevertheless, such US patents were granted.

As a consequence, we believe that the invention contained in the patent in suit, as limited by independent claim 1 as granted following to the European examinations and according to the interpretation outlined in section 4 of the present report, **has the character of inventive step** under Art. 16 Law of

Inventions with respect to the art existing at the time of the priority of the patent in suit.

9) ON THE FOURTH QUERY: INFRINGEMENT

9.1) Micron Devices in suit

Micron devices in suit subject of this query are SDRAM semiconductor memory devices, identified with codes Y95C, Y72C, Y85C, Y84C, which correspond to the commercialization codes MT48LC16M8A2, MT48LC1M16A1, MT48LC16M8A2, MT48LC8M8A2, as it results in the seizure report dated October 18th, 2000 in the file.

As a direct examination of the characteristics of the said SDRAM memories would not be possible in light of the timeframe of the present report, the undersigned will use the datasheets in the file for identified these characteristics, as authorized by Justice Galletti in his order dated November 20th, 2000.

During the first technical meeting Micron filed 4 print-outs baring codes Y15C, Y72G, Y84B, Y85B, that Micron declare correspondent to the mask sets seized on October 18th, 2000.

The undersigned technical experts that the examination of the above mentioned print-outs is ininfluent for the purposes of the present report, and Rambus did not request the examination of the same. These print-outs are available for Micron at Mr. Stucovitz offices.

9.2) Preliminary comments

Using the chart exposed at point 4 regarding the interpretation of the patent, we will proceed verifying whether Micron memories have the same elements of the combination patented by Rambus.

A semiconductor memory device having at least one memory array (1) which includes a plurality of memory cells.	a memory device

Clock receiver circuitry (101, 111) for receiving an external clock signal (53, 54)having a fixed frequency	The memory device is synchronous since it receives a clock signal from the outside.
+) a programmable access-time register for storing a value which	A register storing access time values in a modifiable manner
is representative of a number of clock cycles of the external clock signal (53, 54)	A time delay which is a number of clock cycles
to transpire after which the memory device responds to a read request;	before the output of data, a stored number of clock cycles from the synchronous arrival of the read request has to transpire
a plurality of output drivers (76)	Any driver capable of putting data onto the bus according to a clock signal
for outputting data onto an external bus (18, 65) in response to a read request,	the external bus is at least synchronous
Wherein the output drivers (76) output data on the external bus (18, 65) after the number of clock cycles of the external clock transpire and synchronously with respect to the	The drivers make the data available on the bus after the stored number of cycles of the external clock transpiring from the clock

external clock signal (53, 54).	`signal in which the request is registered.`

9.3.) The data sheets

A semiconductor memory device having at least bank memory array which includes a plurality of memory cells.

From page 1 of the above mentioned data-sheets, edited by Micron Technology in the year 2000, it results that the same are Synchronous RAM semiconductor memory devices.

- See Micron datasheet sent by fax (page 1)

From the chart of page 6 it is possible to ascertain that the device contains a bank memory array.

- See diagram sent by fax (page 2)

The memory device including a circuit of a clock receiver in order to receive an external clock signal having a fixed frequency.

From the same page 1 you learn that the memory is fully synchronous: all signals registered on a positive edge of system clock and that it receives a clock signal CLK in a logic control unit which is defined at page 7 as driven by the clock system, identifying an external clock signal having a fixed frequency.

+ a programmable register of time access to memorize a value which is representative of a number of clock cycles of the external clock signal.

In the figure at page 6 a MODE REGISTER is described. Its function is described at page 8 of the chapter "Register Definition". In this chapter it is explained that the MODE REGISTER is used to define the specific way of functioning of the SDRAM Memory (length, burst type etc.) and specifically the bits M4-M6 define the CAS latency.

To transpire after the memory devices responds to a read request

The CAS latency is defined at page 10 as the delay in clock cycles between the registration of a command of Read and the release of the first element of data. The latency is programmable in 2 or 3 clock ticking.

+ a plurality of elements of output drivers to release data in an external bus in response to a read request.

Again in the same scheme at page 6 it is evident that there are 2 registers respectively of data input and data output similar to the elements of output drivers claimed in the Rambus patent.

This is also confirmed by the presence of a DQM signal which has the function of enabling the release of data (see the truth table 1 at page 11) operating directly on the output register.

In which the elements of output drivers release data on an external clock.

From the figure at page 6 you can see that input and output registers exchange data with a bus indicated as DQO-DQ15.

After the number of clock cycles of the external clock transpire

Again at page 10 you read that, in general, if a read request is registered on the edge of clock n in input and the pre-determined latency in the REGISTER MODE is m clock ticking, the data will be released at the edge of the clock (n+m).

And in a synchronous way in respect to the external clock signal

From the time chart at page 41 READ WITHOUT PRECHARGE which refers to a reading operation with release of data in burst and conedgeing the temporal line DQ relative to the data with temporal line CK relative to the clock, you can see that data in output indicated with m, m+1 etc. have the edge before the rising edge of the clock, but they are valid during the interval tOH (see at page 33 DATA OUT HOLD TIME) coincident with the clock edge. Therefore not only the data are released at the same clock frequency, but also in a stable phase relation.

9.4) INTEGRATIVE COMMENTS

From the above it results that all the elements of the combination claimed in the patent in suit are "literally" present in the documentation which can be considered representative of the memory device seized.

In this respect it is appropriate commenting at least some of the elements in light of the opposed interpretation given by the parties to the undersigned technical experts.

a) LATENCY TIME (CAS latency)

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The use by Micron of a programmable register of time access is limited to the use of a value of CAS latency which substantially define the speed of the external clock, while the time register in the patent has a sustantially different objective, which to modify the access time depending from the type of access); in other words, notwithstanding the claim it is not specified the use of the memorized access time.

b) READ REQUEST

Micron interpreted the term READ REQUEST in the claim as it is required that the read request contains a full address of the requested data.

With this interpretation Micron read request would be different as it does not contain the row addresses but only the column addresses.

However examining the time charts for example at page 41 in light of the chapter OPERATION at page 14 you learn that any read/write request is preceded by a request ACTIVE close to a column address and ends up with a READ REQUEST. This means that in fact the read request is extended to 3 clock cycles between ACTIVE and READ and the row addresses are given before the column addresses.

Not considering the different time sequence of the elements you have also in Micron memories a complete read request, at least equivalent to the read request in the patent.

c) BUS

To the above comments regarding the fact that the patent refers to a memory device which does not necessarily include a bus the undersigned want to add that they believe that the structure of MICRON bus (which is different from the bus patent because of the presence of 3 synchronous bus: 1 for the data, 1 for the controls, 1 for the addresses) instead of a single multiplexed bus as described in the patent, as from the viewpoint of the functioning of a synchronous memory the data, the addresses and the controls must all come from the same memory, must be synchronous, must be internally controlled by the memory and must be released synchronously with the predetermined latency and must be independent

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from the complete architecture of the system external to the memory claimed in the patent.

Therefore the undersigned technical experts believe that the semiconductor memory devices manufactured according the teaching of Micron datasheets in the file and relative to Synchronous SDRAM memories identified with the codes MT48LC1284A2, MT48LC64M8A2, MT48LC32M16A2, shall be considered falling the patent EP 0 525 068 protection scope in suit as defined by the actual independent claim as granted.

10) THE ARGUMENTS OF THE PETITIONER AND THE DEFENDANT

Given the complexity and the extension of the arguments of the parties in suit, a summary of the same could be misleading. Therefore it is preferable to make reference to the full text of the attached briefs for the eventual examination of the same.

It must be pointed out that in its third brief Micron refers to figures, graphics and descriptive parts which do not correspond to anything in the documentation in the file examined by the undersigned.

11) ANSWERS TO THE QUERIES

Considering result of the exam of the documentation in the file and the arguments used in the precedents points the undersigned respond to the queries as follows:

R1) Rambus patent EP 0 525 068 has the requirements of novelty and inventive step which are requested by the Italian Patent Law for its validity.

R2) The invention is described in a manner sufficiently clear and complete that an expert person may implement the invention.

R3) The patent is not extended beyond the content of the original claims.

R4) SDRAM semiconductor memory devices manufactured in accordance with the teaching of Micron DATA Sheets in file and relative to Synchronous memory identified with the codes MT48LC1284A2, MT48LC64M8A2, MT48LC32M16A2 must be considered as falling in the scope of claim 1 as granted of Rambus patent EP 0 525 068.

Milan, April 30th 2001

Dott. Ing. Giorgio Crovini   Dott. Ing. Paolo Stucovitz

List of attachments

1. Report of the first meeting

2. Rambus briefs

3. Micron briefs

4. Micron letter dated April 23rd, 2001

5. Rambus letter dated april 26th, 2001

6. Petition of the technical experts for expenses reimbursement and fee payment.