UNITED STATES COURT OF APPEALS FOR THE FEDERAL CIRCUIT
717 MADISON PLACE, N.W.
WASHINGTON, D.C. 20439

JAN HORBALY
CLERK

TELEPHONE: 633-6550
AREA CODE 202

December 11, 2002
BY FACSIMILE:

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2002 DEC 11 PM 2:47

Re: Rambus Inc. v. Infineon Technologies, 01-1449

Dear Counsel:

The panel assigned to decide this appeal requests that one of the parties inform this court as to whether the JEDEC SDRAM standard is part of the trial record, and if so, provide the court with any portions of the SDRAM standard discussing: 2-bank SDRAM designs, externally supplied reference voltage, phase lock loops, programmable CAS latency, and programmable burst length. Additionally, one of the parties should provide this court with the complete prosecution history for U.S. Patent Application Serial No. 07/510,898.

These documents are urgently needed by the panel; therefore, we request that you provide this information as soon as possible. Both parties need not provide the same information.

If you have any questions regarding this request, please contact Supervisory Deputy Clerk Linda Purdie or Senior Deputy Clerk Karen Smagala Hendrick at 202-312-5523.

Sincerely,

Jan Horbaly

Jan Horbaly
Clerk

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