Technology and Manufacturing

Laurent Bosson
Executive Vice President
Technology
## Technology Development Centers and Main Programs

<table>
<thead>
<tr>
<th>CMOS Logic Platform (Crolles)</th>
<th>Power Management, High Voltage, Embedded NVM and MEMS</th>
</tr>
</thead>
<tbody>
<tr>
<td>- 300mm Alliance</td>
<td>Agrate (8”)</td>
</tr>
<tr>
<td>- 65nm process qualified, prototyping started</td>
<td></td>
</tr>
<tr>
<td>- Convergence of RF/Analog Mixed Signal in 65nm</td>
<td></td>
</tr>
<tr>
<td>- 45nm in development</td>
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<tr>
<td>- 32nm under definition</td>
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<tr>
<td>- Embedded DRAM</td>
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</table>

<table>
<thead>
<tr>
<th>CMOS Analog Platforms</th>
<th>NV - Memory Platforms (Agrate)</th>
</tr>
</thead>
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<tr>
<td>- ST Crolles</td>
<td>- NOR:</td>
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<tr>
<td>- RF Receiver/Transmitter technologies</td>
<td>- 65nm in qualification</td>
</tr>
<tr>
<td>- Imaging technologies</td>
<td>- 45nm in development</td>
</tr>
<tr>
<td></td>
<td>- Phase Change Memory</td>
</tr>
<tr>
<td></td>
<td>- NAND JV with Hynix, New 12” in China</td>
</tr>
</tbody>
</table>
High Performance Logic Technologies in Crolles 2

- **CMOS 65 nm**
- **CMOS 45 nm**: Advanced R&D
- **CMOS 32 nm**: Advanced R&D
- **CMOS 22 nm**: Advanced R&D

1st Silicon

Prototypes

Start Production

Base logic technologies are design rule aligned with Foundry Partners
65nm: Qualified Technology

- Next generation platform for Set Top Box
  - > 100 million transistors
  - > 800 pads
  - Several million lines of SW code
  - VLIW ST231 core, ST40 CPU core
  - Advanced Digital Rights Management

- Market: dual advanced codecs High Definition decoder
  - iDTV with advanced codecs
  - Dual TV STBs
  - Media Servers
  - HD-DVD and Blu-Ray capable
  - High-end IPTV

- Single chip solution

65nm product
Sampling mid-06
Production ramp-up H107
Crolles2 Technology Pipeline from Advanced Research Institutes

Materials and Advanced Modules

45nm Design Rule Inputs

45nm Device Architecture

Stressor Technologies

Gate Stack (High-k, M-Gate)

E-beam Direct Write Litho

BEOL Materials & Integration

Immersion Lithography

Crolles Narrowed Options

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45nm Technology Development

- **Status:**
  - 300mm equipment and process available
  - Complex test chip running
  - Device performance demonstrated
  - Scheduled for production early 2008

- **Advanced Process Features:**
  - Very high NA Immersion lithography
    - Minimum pitch = 130nm
  - Optimized NiSi Salicide
  - Extensive use of stressors for mobility improvement
  - Very low k (2.6) intermetal dielectric integration
  - Design rules adapted for better manufacturability
  - Design solutions for power management
32nm Technology Research

**Status:**
- 300mm equipment available for feasibility demonstration
  - Use of e-beam direct write for minimum dimension
- SRAM 0.124µm² process
- Scheduled for production early 2010

**Advanced Process Features:**
- High k and metal gate technology
- Junctions’ laser annealing
- Ultra low k (2.3) intermetal dielectric
- Self-aligned barriers
- Innovative SRAM solutions study
High Performance Logic Program

### Prototypes

Normalized N° of prototypes

<table>
<thead>
<tr>
<th>Year</th>
<th>120 nm</th>
<th>90 nm</th>
<th>65 nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>2001</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>2002</td>
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<td>2005</td>
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</tr>
<tr>
<td>2006</td>
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</table>

#### 2006 Status

<table>
<thead>
<tr>
<th>Technology</th>
<th>Production</th>
<th>Qualification</th>
<th>Development</th>
</tr>
</thead>
<tbody>
<tr>
<td>CMOS</td>
<td>90nm</td>
<td>65nm</td>
<td>45nm</td>
</tr>
<tr>
<td>Embedded DRAM</td>
<td>120nm</td>
<td>90nm</td>
<td>65nm</td>
</tr>
</tbody>
</table>

#### 2011 Projection

<table>
<thead>
<tr>
<th>Technology</th>
<th>Production</th>
<th>Qualification</th>
<th>Development</th>
</tr>
</thead>
<tbody>
<tr>
<td>CMOS</td>
<td>45nm</td>
<td>32nm</td>
<td>22nm</td>
</tr>
<tr>
<td>Embedded Memory</td>
<td>45nm</td>
<td>32nm</td>
<td>22nm</td>
</tr>
</tbody>
</table>

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Embedded Flash

- Over 10 years experience through 5 technology generations and volume manufacturing for automotive and consumer electronics
- Flash know-how based on stand-alone memory products:
  - memory cell
  - memory block design and testing
  - process modules and manufacturing control
- Modular process flow to ensure:
  - Core CMOS compatibility for IP reuse
  - Flash memory yield and reliability
- Production running in the same fabs as stand-alone Flash

- 180 nm
  - 0.37 µm² Flash cell

- 90 nm
  - 0.18 µm² Flash cell

- 65 nm
  - 0.10 µm² Flash cell

Prototypes: Q2/02 Q1/07 H2/08
# Non Volatile Memory Processes

## Q2 2006 Status / Programs

<table>
<thead>
<tr>
<th></th>
<th>Production</th>
<th>Qualification / Production Start</th>
<th>Development</th>
<th>Key Applications</th>
</tr>
</thead>
<tbody>
<tr>
<td>Flash NOR 2 bit / cell</td>
<td>90nm</td>
<td>65nm</td>
<td>45nm</td>
<td>Mobile Phones Code Storage</td>
</tr>
<tr>
<td>Flash NAND</td>
<td>70nm</td>
<td>60nm</td>
<td>50nm</td>
<td>Mobile Phones Data Storage</td>
</tr>
<tr>
<td>Embedded Flash</td>
<td>0.18µm</td>
<td>-</td>
<td>90nm</td>
<td>Automotive</td>
</tr>
<tr>
<td>Smart Cards</td>
<td>0.15µm</td>
<td>0.13µm</td>
<td>90nm</td>
<td>Smart Cards</td>
</tr>
<tr>
<td>E PROM / flash</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
NOR Flash Roadmap

Prototypes:
- Q1/03
- Q3/04
- Q4/05
- Q4/07
- H1/10

Technology Nodes:
- 130 nm: 0.16 µm²
- 90 nm: 0.076 µm²
- 65 nm: 0.042 µm²
- 45 nm: 0.024 µm²
- 32 nm: 0.015 µm²

Memory Cell:
- 0.042 µm²

Other Points:
- 512Mb 1.8V Multibank 2 bit/cell
NAND Flash Roadmap

Prototypes:
- Q2/04
- Q2/05
- Q2/06
- Q2/07
- H2/08

- 90 nm, 0.038 μm²
- 70 nm, 0.021 μm²
- 60 nm, 0.015 μm²
- 50 nm, 0.01 μm²
- 42 nm, 0.007 μm²

4 Gbit
Preparing for the Future

- **Pushing the limits of flash memories**
  - Evolutionary development for 45nm feasible
  - Investigation of innovative solutions for 32nm

- **Accelerating the activity on phase change memory**
  - Product development and technology industrialization in progress
  - Addressing both stand-alone and embedded memory

- **Structuring the activity on probe storage (MEMS based memory devices)**
  - Kicked-off the internal development program
  - Joint development program with key partners under definition
ST Phase Change Memory Roadmap

Maturity

Technology Demonstrator
- Cell performances
- Statistics
- Reliability

Large Array Demonstrator
- Prod. performances
- Bandwidth
- Endurance
- Manufacturability
- Cost
- Scaling

Volume Production
- System spec.
- nGbit density
- Bandwidth
- Cost

Technology Node (nm)
- 180
- 90
- 45-32

Years
- 02-04
- 05-07
- >08

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BCD / High Voltage Gate (HVG) Product Fields

A wide variety of applications covering a large voltage range

- 700V
  - AUTOMOTIVE
  - INDUSTRIAL
  - CONSUMER
  - TELECOM
  - HIGH VOLTAGE BCD
- 200V
  - AUTOMOTIVE
  - INDUSTRIAL
  - HIGH POWER BCD
- 100V
  - AUTOMOTIVE
  - INDUSTRIAL
  - HIGH DENSITY BCD
- 80V
  - AUTOMOTIVE
  - INDUSTRIAL
- 60V
  - DISPLAY
  - CONSUMER
  - HARD DISK DRIVE
  - HVG

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BCD / HVG Process Roadmap
(3 Gate Oxide)

HVG6s (0.32 µm)
3.3V/5V CMOS
25V/40V MOS

HVG8 (0.18 µm)
1.8V/5V CMOS
20V/32V/40V MOS

HVG9S (0.11 µm)
1.2V/5V CMOS
20V/32V/40V MOS

HVG10 (0.09 µm)
1.2V/3.3V CMOS
20V/32V/40V MOS

Videophone: 320RGBx240, ram-less, 17.75x1.19=21.12 mm²

Picture Phone: 240RGBx320, 16.7 Mcolors, 15.81x1.52=24.03 mm²

LCD: 162RGBx132, 262Kcolors, 17.74x1.24=22.07 mm²

2004 2006 2007 2009
System in Package (SiP)
Integration Technologies

- Memory + Memory
- ASIC + Memory
- Stack Dice
- Package on Package (POP)
- Package in Package (PIP)

SYSTEM
- Multichip
- Passives
- III-V
- MEMS
- Sensors

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Beyond SoC, SiP

- Stacked dice

- Modules and Integrated Passive Devices
- High volume wireless applications
Stacked BGA: 8 Die + 7 Interposers
(Package Height = 1.6mm)

Thickness:
- Package: 1.6mm
- Die: 40 µm
- Interposer: 40 µm

4.5 years faster than Moore’s Law
Manufacturing
<table>
<thead>
<tr>
<th>6”</th>
<th>8” System Oriented</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ang Mo Kio (Singapore)</td>
<td>Agrate (Italy)</td>
</tr>
<tr>
<td>Carrollton (Texas)</td>
<td>Ang Mo Kio (Singapore)</td>
</tr>
<tr>
<td>Catania (Italy)</td>
<td>Crolles 1 (France)</td>
</tr>
<tr>
<td>Tours (France)</td>
<td>Phoenix (Arizona)</td>
</tr>
<tr>
<td></td>
<td>Rousset (France)</td>
</tr>
</tbody>
</table>

**NV Memories**
- Agrate (Italy)
- Ang Mo Kio (Singapore)
- Catania (Italy)
- ST-Hynix JV in Wuxi (China)

**12” Advanced Logic**
- Catania M6 (Italy)
  - Ready for clean room
- Crolles 2 Alliance (France)

+ Foundry Partnership Agreements
CMOS LOGIC <= 0.13µ - Wafer Outs
(8” Equivalent)

Q1 2005

58% Internal
42% External

Q1 2006

47% Internal
53% External
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CMOS LOGIC \(< 0.13\mu\) - Wafer Outs

(8” Equivalent)

Three 300 mm & three 200 mm Fabs qualified
Critical mass
- 1200 people, 600 researchers
- Cumulative Capex: $1.6B by mid-2006

Technology leadership
- 12"
- Technology node: from 120 nm to 22 nm
- 2500 wafer starts per week in Q3 2006
- Opportunity to expand full build out capacity
Crolles 2 Manufacturing Mix Evolution

120nm to 90nm Ratio

Jan-05  Mar-05  May-05  Jul-05  Sep-05  Nov-05  Jan-06  Mar-06

- 120 nm
- 90 nm
Singapore Technopark - 8” Equivalent Wafers (% output of total internal capacity)


Base 100 Q4 2005

Singapore %  Others %
8” System Oriented Fabs
Asset Utilization Leverage

Wafer starts / quarter

Q4 2003
Q4 2004
Q4 2005
Q4 2006e

BASE 100 Q4 2003

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Flash Manufacturing

NOR Flash
- Volume production in 130nm of 2-bit per cell and 110nm 1-bit per cell at Singapore and Catania respectively
- Production of 90nm 2-bit per cell currently at Agrate/R2 and ramping-up in Singapore
- 65nm in qualification and 45nm in development at Agrate/R2

NAND Flash
- Volumes in 70nm from Hynix partnership
- Prototyping 60nm and developing 50nm in collaboration with Hynix
- Completing ST-Hynix JV new Fab in Wuxi, China
Cost Reduction Initiatives
(Depreciation Rollover* and 8” & 12” Improvements)

- Double-digit wafer cost reduction in 8” and 12” target from Q106 to Q406
  - Approximately 2/3 of savings due to depreciation rollover
  - Approximately 1/3 of cash savings from manufacturing efficiencies
- $100+ million of additional reduction in depreciation in 2007

### Total Depreciation

- ‘05: $1,846M
- ’06: $1,700M

### 8” & 12” Wafer Cost Reduction

*Based on approximate 1.25 Euro / $ rate and does not imply any guidance on 2007 CapEx

Front-End Technology and Manufacturing

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Conclusion

- ST’s Technology and Manufacturing Machine supports our customer base through product innovation and efficient manufacturing.

- The consolidation of the 6” Manufacturing Machine in Singapore offers a dimension of scale that enables low cost and reliable manufacturing along with the rapid introduction of new products.

- ST’s 8” system oriented technologies and Fabs are taking full advantage of new developments in high performance logic.

- ST’s flexible and responsive manufacturing structure is complemented with foundry partnerships to better serve our customer’s needs by providing a stronger product pipeline.

- CMOS Logic Advanced Technologies well-balanced between internal & external capacity.

- A strong and motivated R&D/Manufacturing team is in place.