Physical IP Overview

May 2006

Cautionary Statement Concerning Forward-Looking Statements

- This presentation contains forward-looking statements as defined in section 102 of the Private Securities Litigation Reform Act of 1995. These statements are subject to risk factors associated with the semiconductor and intellectual property businesses. When used in this document, the words “anticipates”, “may”, “can”, “believes”, “expects”, “projects”, “intends”, “likely”, similar expressions and any other statements that are not historical facts, in each case as they relate to ARM, its management or its businesses and financial performance and condition are intended to identify those assertions as forward-looking statements. It is believed that the expectations reflected in these statements are reasonable, but they may be affected by a variety of variables, many of which are beyond our control. These variables could cause actual results or trends to differ materially and include, but are not limited to: failure to realize the benefits of our recent acquisitions, unforeseen liabilities arising from our recent acquisitions, price fluctuations, actual demand, the availability of software and operating systems compatible with our intellectual property, the continued demand for products including ARM’s intellectual property, delays in the design process or delays in a customer’s project that uses ARM’s technology, the success of our semiconductor partners, loss of market and industry competition, exchange and currency fluctuations, any future strategic investments or acquisitions, rapid technological change, regulatory developments, ARM’s ability to negotiate, structure, monitor and enforce agreements for the determination and payment of royalties, actual or potential litigation, changes in tax laws, interest rates and access to capital markets, political, economic and financial market conditions in various countries and regions and capital expenditure requirements.
- More information about potential factors that could affect ARM’s business and financial results is included in ARM’s Annual Report on Form 20-F for the fiscal year ended December 31, 2004 including (without limitation) under the captions, “Risk Factors” and “Management’s Discussion and Analysis of Financial Condition and Results of Operations,” which is on file with the Securities and Exchange Commission (the “SEC”) and available at the SEC’s website at www.sec.gov.

Contents

- The Physics Behind Physical IP
- Market Drivers for Physical IP
- Financial Models for ARM Phyiscal IP

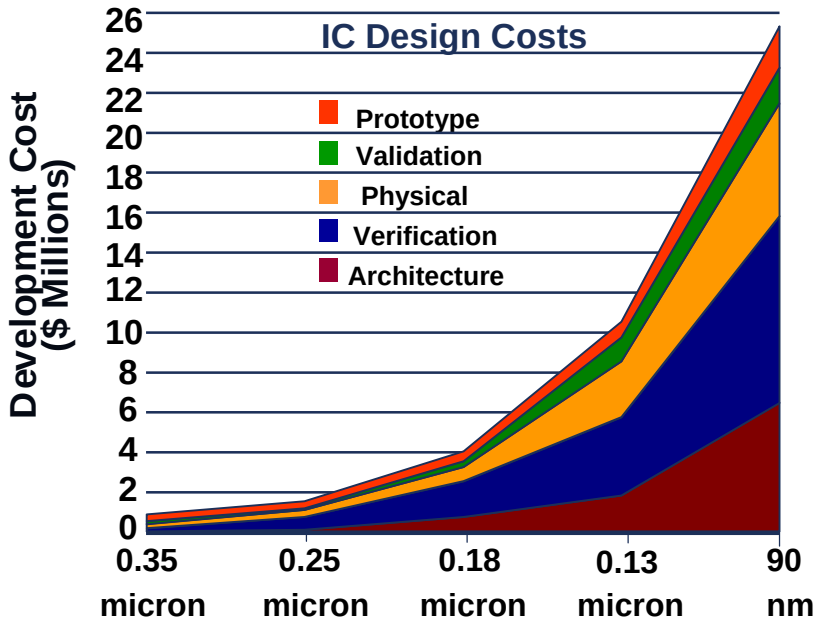
The Physics Behind Physical IP

Brent Dichter

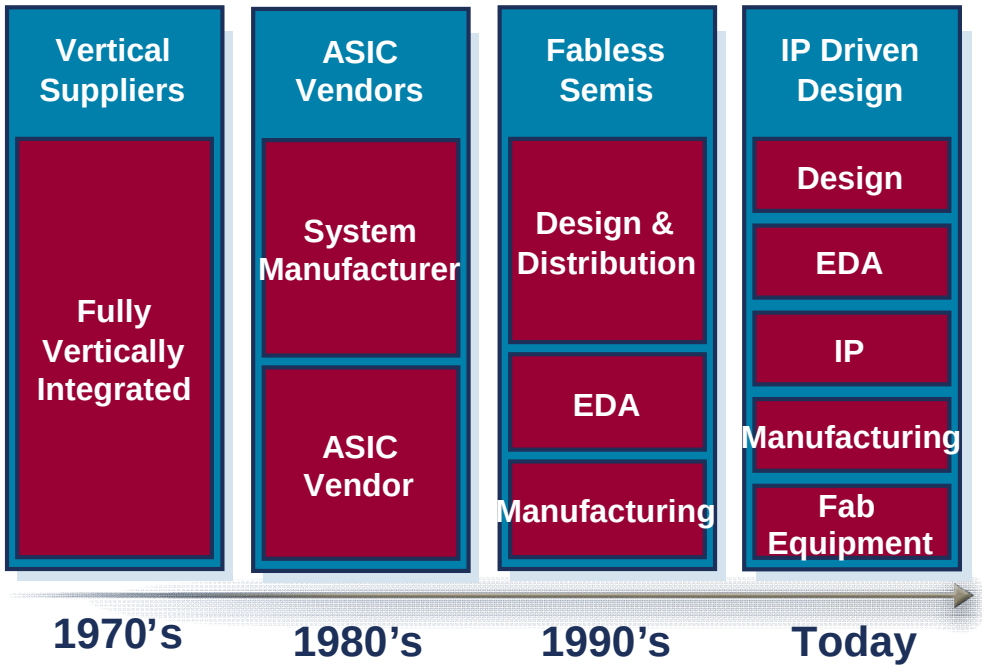
GM, Physical IP Division

Semiconductor Industry – A history of Outsourcing

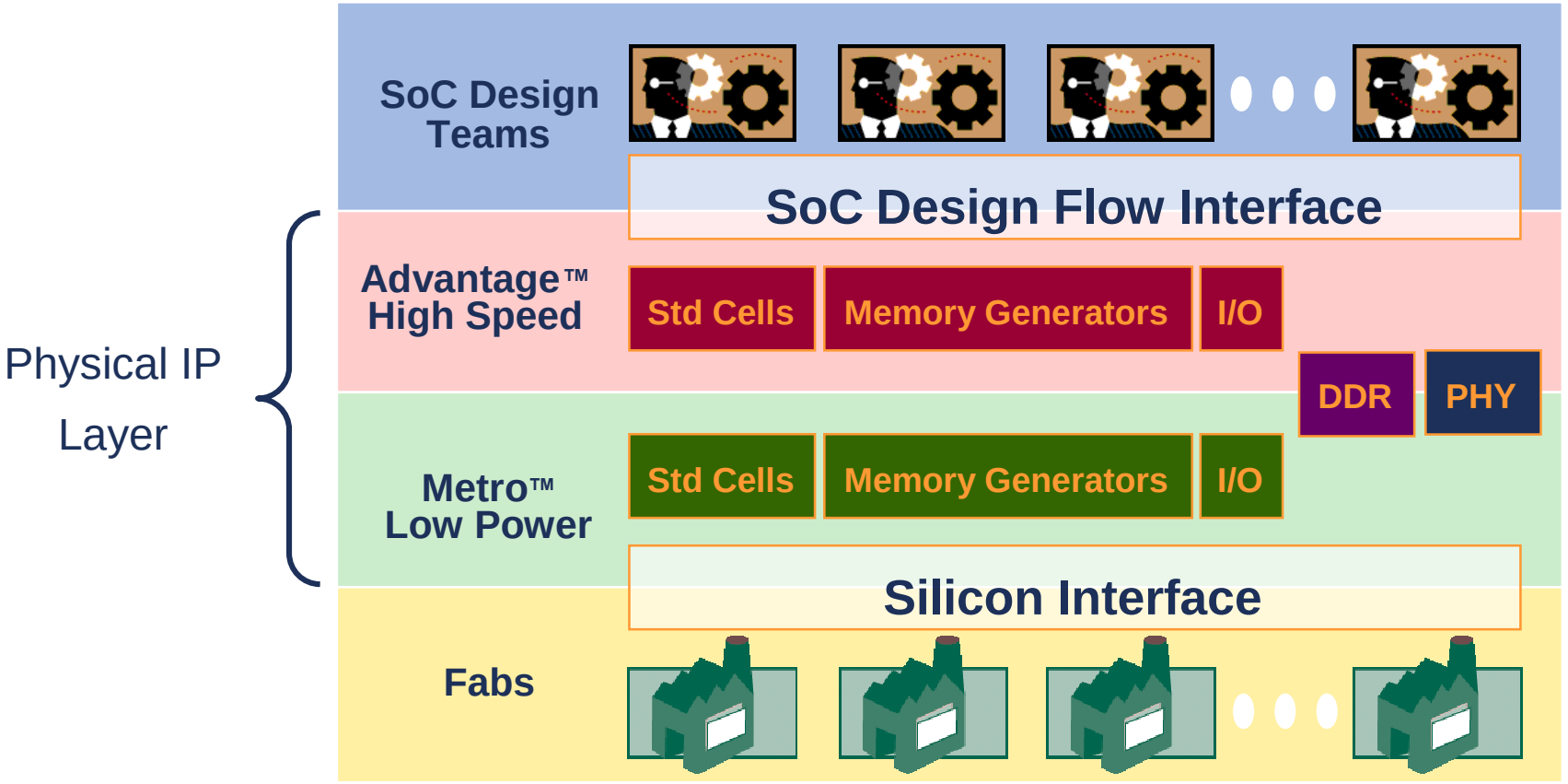
- Technical progress brings a basis for industry evolution
  - Miniaturisation, reduction in chip costs, increase in complexity
- Increased complexity has exponential effect on design costs
- Rising costs give way to specialisation and outsourcing



Source: International Business Strategies



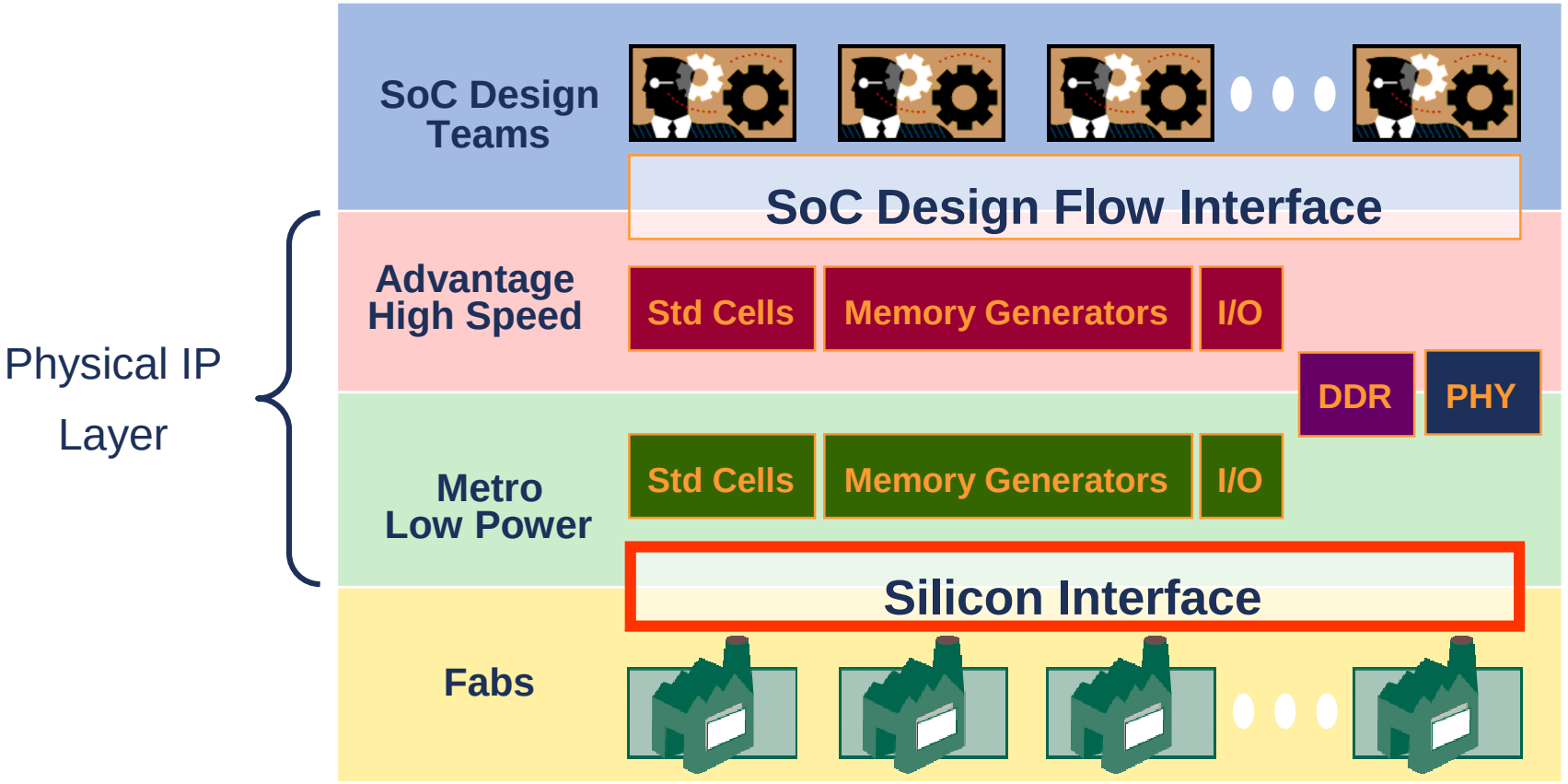
Physical IP Layer



Rising Complexity

- Complexity of basic structures rises at each process node
  - At all levels
- Physical level – feature sizes reach atomic levels
  - Transistors become a few atoms thick
  - Line-widths become less than wavelength of light
  - Tiny impurities can have a devastating effect
- System level
  - More interfaces and “views” needed to operate with EDA environment
- Practical level
  - Dramatically more compute power needed to validate each element
- A library of structures doesn’t just have to work
  - It needs to be tolerant to manufacturing challenges
- “Good” library development has new dimensions
  - Has a major impact on yield – manufactured costs

Silicon Interface

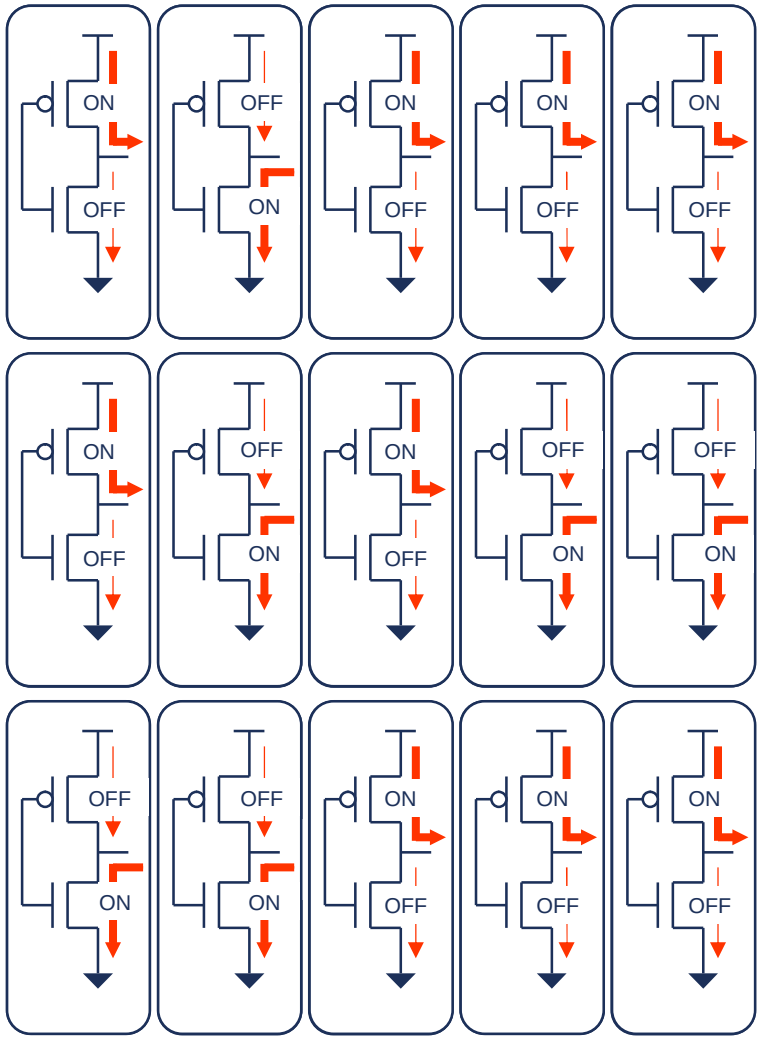


Meeting Future Challenges

	180nm	130nm	90nm	65nm	45nm
Performance	✓	✓	✓	✓	✓✓
Area	✓	✓	✓	✓	✓✓
Dynamic Power	✓	✓	✓	✓	✓✓
Static Power		✓	✓	✓	✓✓
DFM			✓	✓	✓✓
Device Variability				✓	✓✓

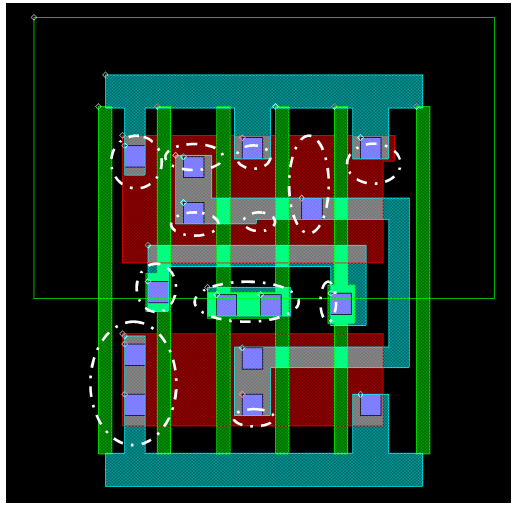
“Leakage”

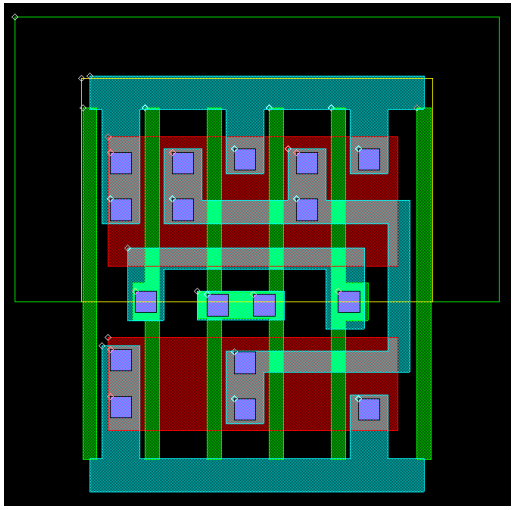
- Devices do not completely turn ‘off’ and ‘leak’ electrons
  - Analogous to a faucet that drips even when turned ‘off’
  - One leaky faucet not a big deal
  - Millions of leaky faucets would waste millions of gallons hourly
- ‘Leaky’ transistors
  - Reduce battery life
  - Larger, more expensive power supplies
  - Expensive packages
  - Long-term reliability reduction
  - Leakage increasing with each process generation
  - Leakage now measured in amps for many chips (versus milliamps a decade ago)
- Physical IP
  - Architecture/Circuit innovation to minimise or tolerate leakage increase



DFM – Design For Manufacturability

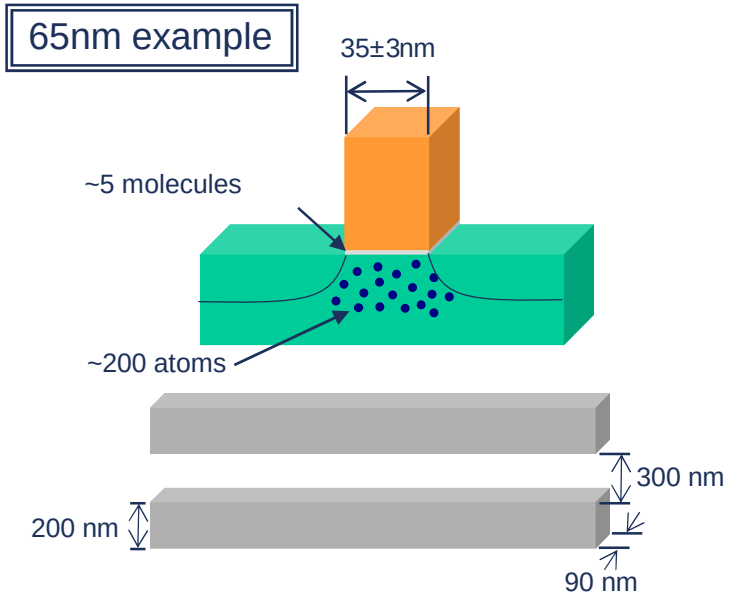
- Things that need to be done to increase amount of working silicon…
- Why needed?
  - Printability worsens as feature sizes shrink and exposure wavelengths remain constant
  - Narrower interconnect layers and reduced depth of focus lead to greater variability
- Layout must comprehend yield issues
  - Manufacturing ‘friendly’ layout
  - Even pattern density
  - Structure redundancy (contacts and vias)
  - Use of non-minimum rules
- Repairability
  - **Memories must be testable and repairable**
  - **Built-In Memory Test and Repair**

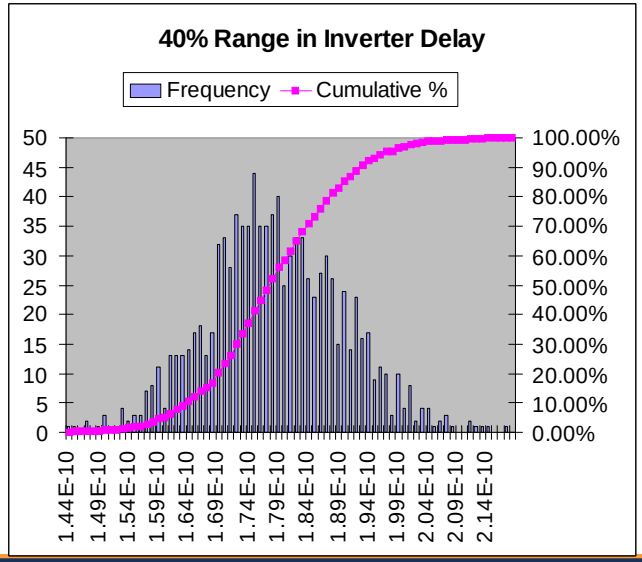




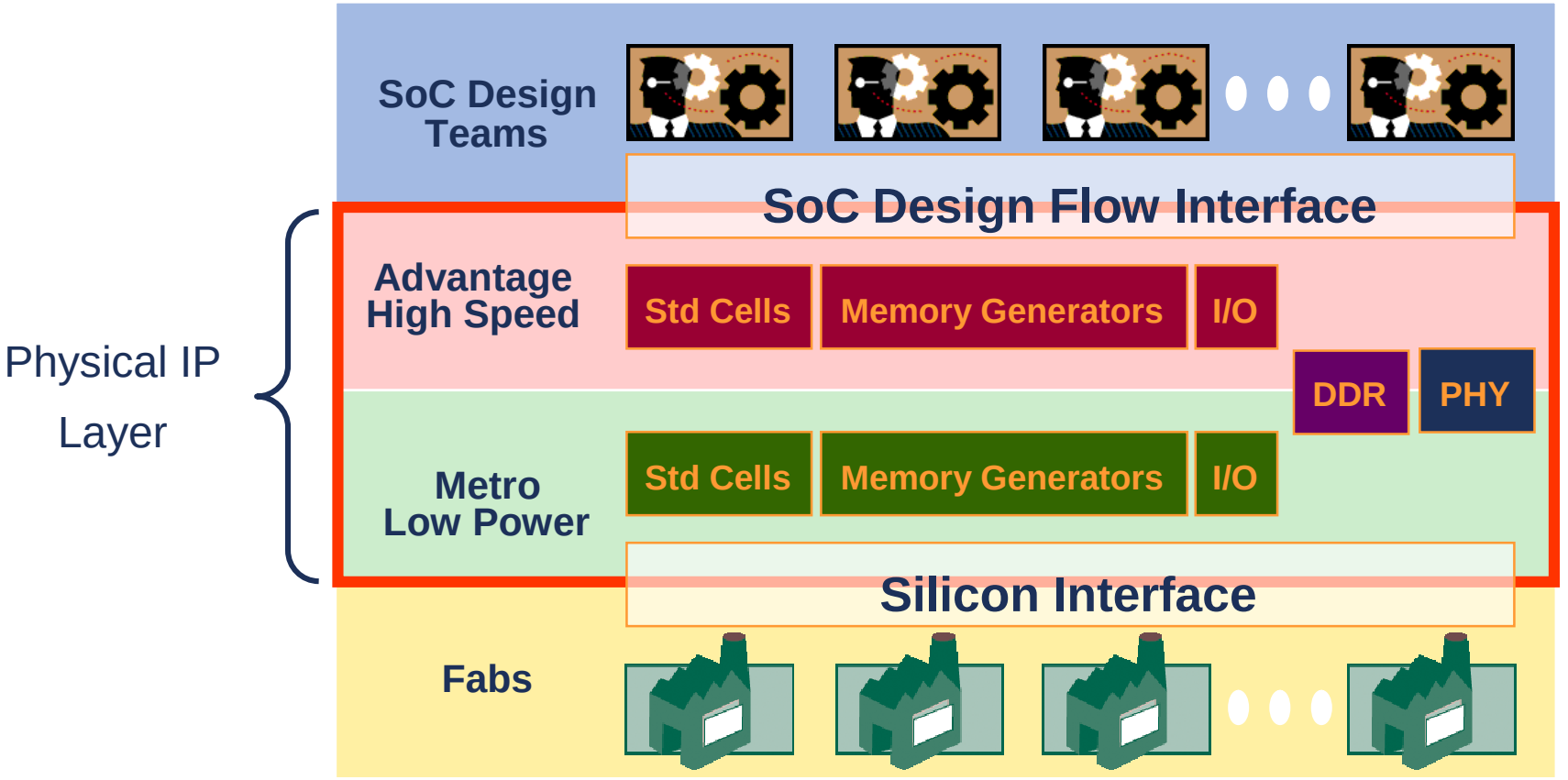
Device Variability Considerations

- Transistor variations
  - Channel Dopant Atoms
  - Gate Oxide thickness
  - Channel width
- Interconnect variations
  - Wiring widths, thicknesses, spacing
  - Edge roughness, rounding
- The Problem
  - On-Chip variation percentage growing
- The Solution
  - Statistical analysis
  - Variation tolerant circuits and layouts
  - Design centering and margining



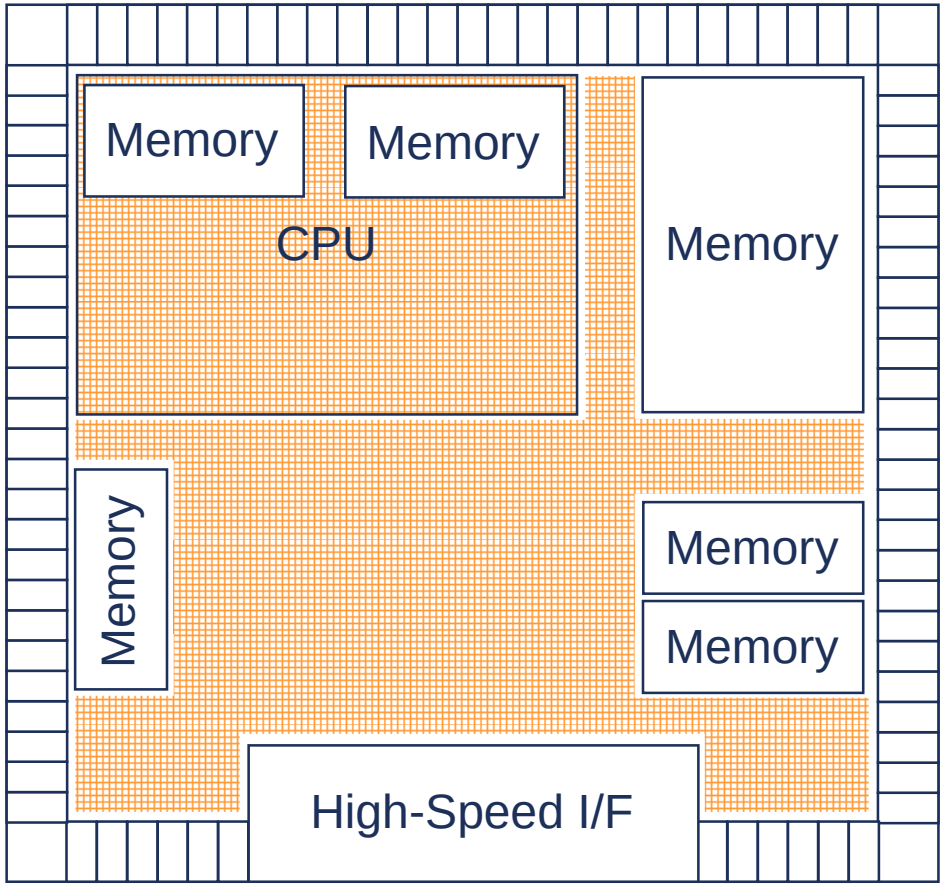


Physical IP Layer



Physical IP SoC Building Blocks

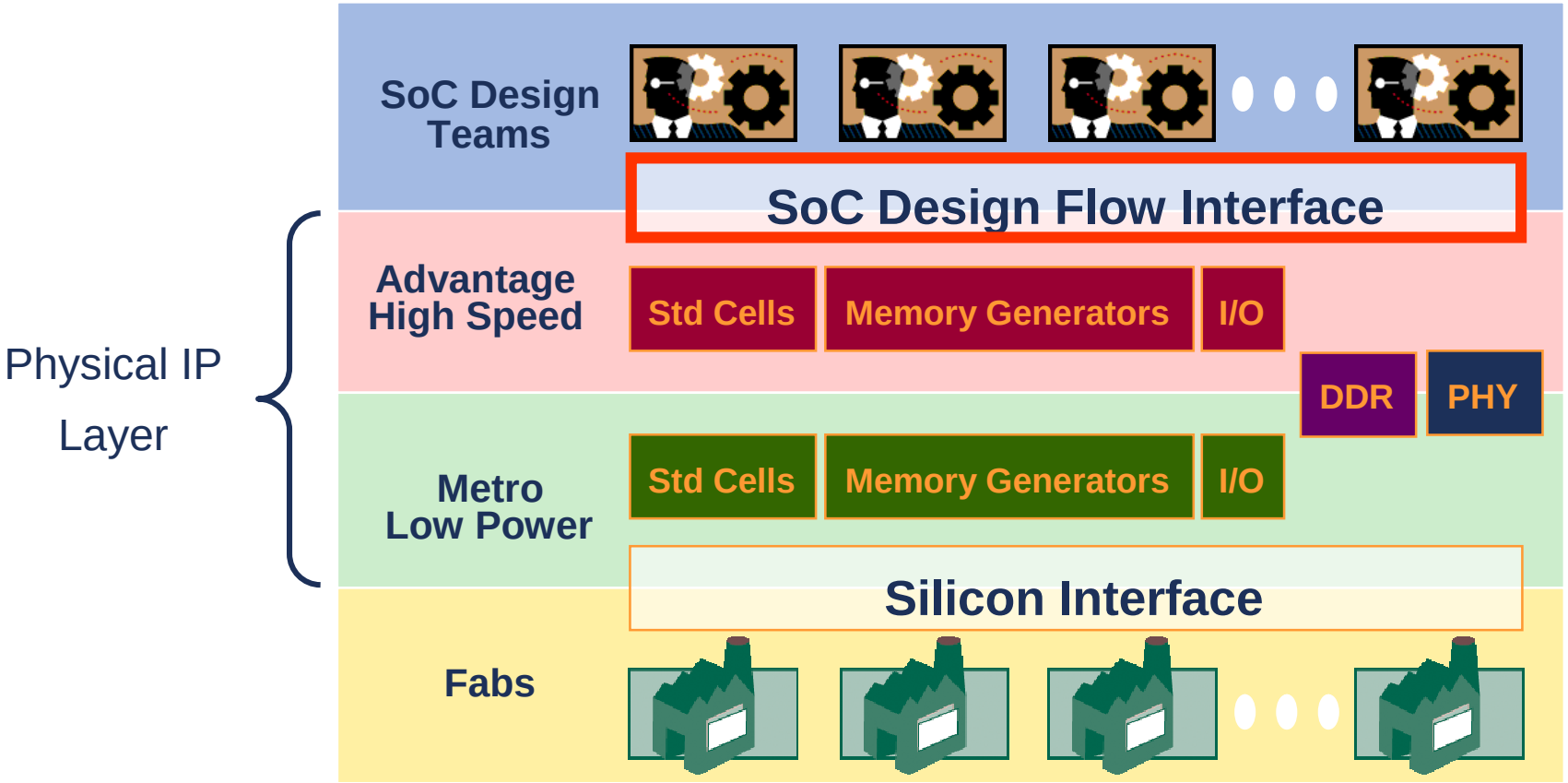
- I/O Cells
  - Communicate to “outside” world
  - Protect the “insides” of the chip from “outside” world
- High-Speed Interfaces
  - Serial Interfaces (PCI Express)
  - Memory Interfaces
- Standard Cells
  - Perform the “logic” function of the SoC (x, /, -, +)
  - Storage of ‘bits’ of information
- Memories
  - Storage for large amounts of information
- CPUs
  - Comprised of Physical IP blocks



ARM's Artisan® Physical IP Platforms

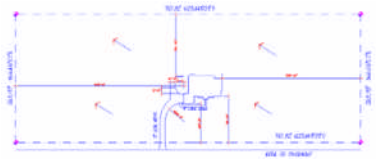
***Classic Mainstream Platform	ADVANTAGE™ Performance Platform	METRO™ Low-Power Platform	VELOCITY™ High-Speed PHYs
SAGE-X™ Standard Cell	Advantage™ Standard Cell	Metro™ Standard Cell	PCI-Express
Single/Dual Port SRAM	Single/Dual Port SRAM	Single/Dual Port SRAM	Serial-ATA
1/2-Port Register File	1/2-Port Register File	1/2-Port Register File	XAUI
ROM Via or Diffusion	ROM Via or Diffusion	ROM Via or Diffusion	DDR/DDR2/GDDR3
GPIO Inline/Staggered	GPIO Inline/Staggered	GPIO Inline/Staggered	
Power Management Kit	Power Management Kit	Power Management Kit	
Analog/Mixed Signal PLLs, DLLs Specialty I/Os	Analog/Mixed Signal PLLs, DLLs Specialty I/Os	Analog/Mixed Signal PLL, VREG, OSC, Specialty I/Os	

SoC Design Flow Interface

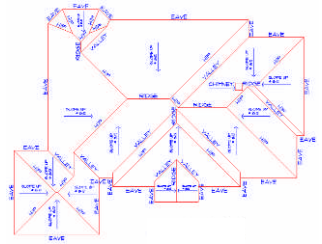


House Plan “Views”

Plot Plan

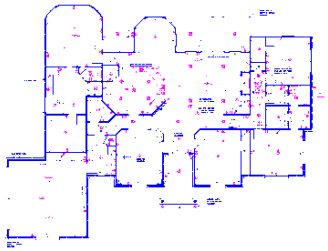


Roof Plan

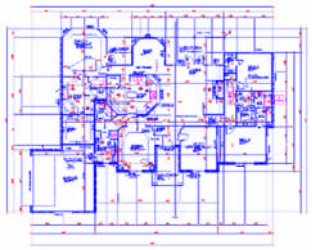


Front Elevation

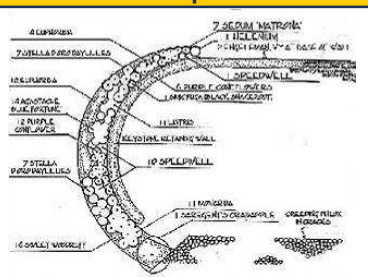
Electrical Plan



Floorplan



Landscape Plan



Physical IP EDA “Views”

Synthesis

```
cell (NAND2X1MTH) {
  cell_footprint : nand2;
  area : 1.280000;
  pin(A) {
    direction : input;
    capacitance : 0.001149;
  }
  pin(B) {
    direction : input;
    capacitance : 0.001041;
  }
  pin(Y) {
    direction : output;
    capacitance : 0.0;
    function : "!(!A B1)";
    timing() {
      related_pin : "A";
      timing_sense : negative_unate;
      cell_rise(delay_template_7x7) {
        index_1 ("0.032, 0.07, 0.146, 0.296, 0.598, 1.2, 2.406");
        index_2 ("0.0005235, 0.0018846, 0.0046068, 0.0099465, 0.0207306, 0.0422988, 0.0854352");
        values ( \
          "0.043172, 0.063486, 0.102233, 0.180645, 0.336651, 0.648546, 1.272190", \
          "0.057182, 0.077540, 0.117430, 0.194952, 0.351038, 0.662893, 1.286600", \
          "0.083644, 0.104257, 0.144078, 0.222691, 0.379415, 0.691769, 1.315390", \
          "0.129861, 0.150855, 0.190531, 0.269521, 0.426865, 0.738712, 1.372330", \
          "0.195455, 0.216364, 0.311350, 0.397127, 0.552297, 0.863952, 1.497260", \
          "0.289831, 0.369412, 0.474826, 0.608808, 0.784957, 1.094590, 1.717330", \
          "0.419896, 0.546005, 0.717916, 0.930628, 1.206540, 1.562090, 2.191040");
      }
```

Simulation

```
`timescale 1ns/1ps
`celldefine
module NAND2X1MTH (Y, A, B);
output Y;
input A, B;

  nand (Y, A, B);

  specify
    // delay parameters
    specparam
      tplh$A$Y = 1.0,
      tphl$A$Y = 1.0,
      tplh$B$Y = 1.0,
      tphl$B$Y = 1.0;

    // path delays
    (A *> Y) = (tplh$A$Y, tphl$A$Y);
    (B *> Y) = (tplh$B$Y, tphl$B$Y);
  endspecify

endmodule // NAND2X1MTH
`endcelldefine
```

Test

```
module NAND2X1MTH (Y, A, B);
    input A, B;
    output Y;
    nand    I0 (Y, A, B);
endmodule
```

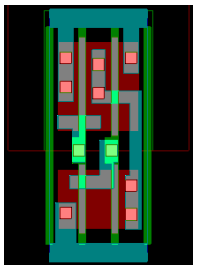
Place and Route

```
MACRO NAND2X1MTH
     CLASS CORE ;
     FOREIGN NAND2X1MTH 0.000 0.000  ;
     ORIGIN 0.000 0.000 ;
     SIZE 0.800 BY 1.600 ;
     SYMMETRY x y ;
     SITE cmos10lpsite ;
     PIN Y
          DIRECTION OUTPUT ;
          PORT
          LAYER M1 ;
          RECT  0.650 0.195 0.750 1.170 ;
          RECT  0.570 0.195 0.650 0.355 ;
          RECT  0.470 1.080 0.650 1.170 ;
          RECT  0.310 1.080 0.470 1.415 ;
          END
          AntennaDiffArea 0.125 ;
     END Y
```

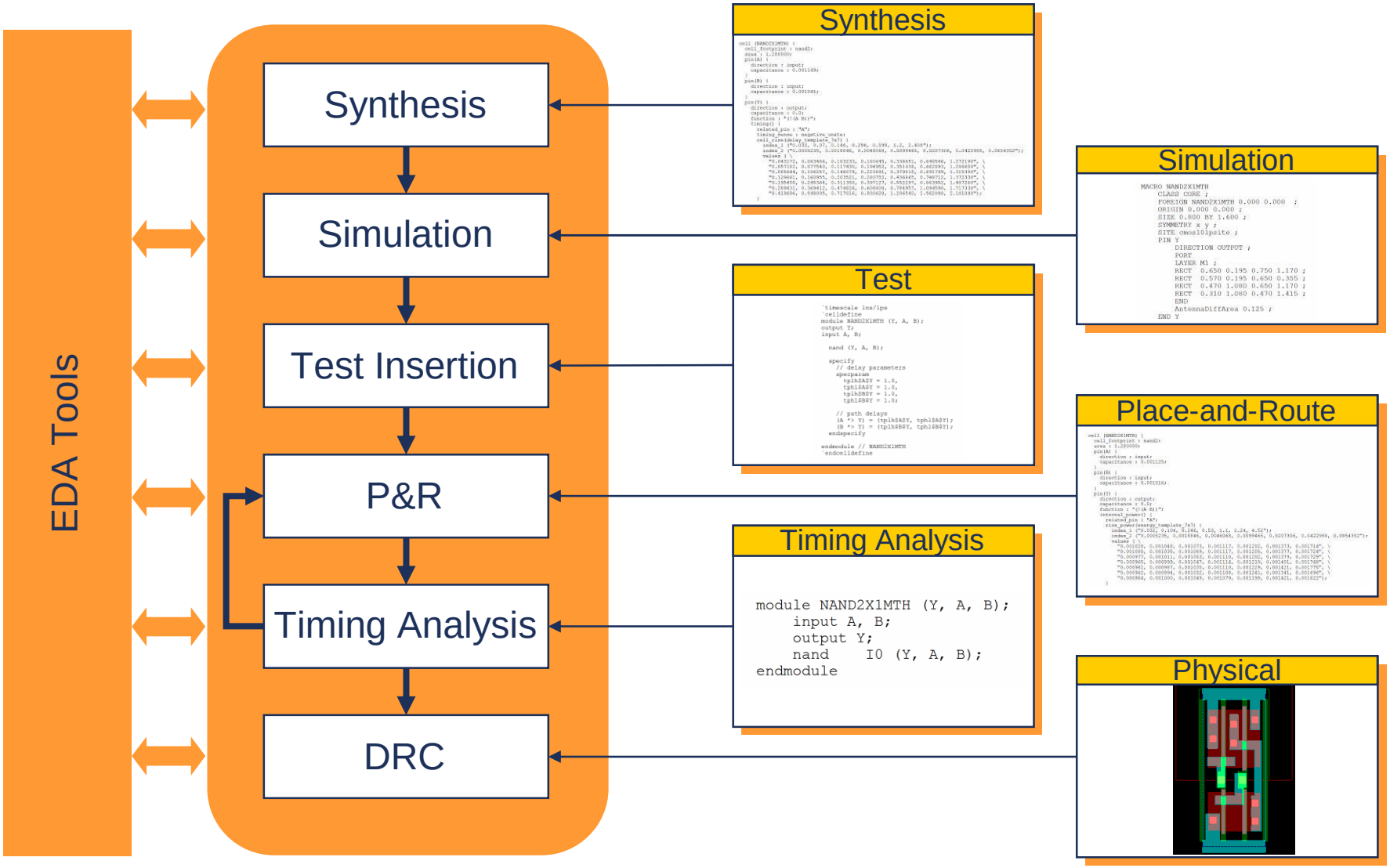
Timing Analysis

```
cell (NAND2X1MTH) {
  cell_footprint : nand2;
  area : 1.280000;
  pin(A) {
    direction : input;
    capacitance : 0.001125;
  }
  pin(B) {
    direction : input;
    capacitance : 0.001016;
  }
  pin(Y) {
    direction : output;
    capacitance : 0.0;
    function : "!(!A B1)";
    internal_power() {
      related_pin : "A";
      rise_power(energy_template_7x7) {
        index_1 ("0.032, 0.104, 0.246, 0.53, 1.1, 2.24, 4.52");
        index_2 ("0.0005235, 0.0018846, 0.0046068, 0.0099465, 0.0207306, 0.0422988, 0.0854352");
        values ( \
          "0.000328, 0.001048, 0.001073, 0.001117, 0.001202, 0.001378, 0.001714", \
          "0.000905, 0.001058, 0.001069, 0.001117, 0.001205, 0.001377, 0.001714", \
          "0.000977, 0.001011, 0.001053, 0.001115, 0.001202, 0.001379, 0.001729", \
          "0.000965, 0.000999, 0.001047, 0.001114, 0.001219, 0.001401, 0.001748", \
          "0.000961, 0.000987, 0.001035, 0.001110, 0.001229, 0.001421, 0.001775", \
          "0.000962, 0.000994, 0.001032, 0.001108, 0.001241, 0.001341, 0.001696", \
          "0.000944, 0.001000, 0.001049, 0.001078, 0.001199, 0.001421, 0.001822");
      }
```

Physical



SoC Design Flow



Summary

- Physical IP layer
  - Closely linked to process technology
  - “Hides” process complexity from SoC design teams
  - Provides EDA “Views” required by SoC design flows
- Advanced process technology challenges
  - Transistor leakage
  - DFM
  - Device variability
- Multiple Physical IP platforms required
  - Metro Area/Power Optimised Libraries
  - Advantage Performance Optimised Libraries
  - CPU Optimised Libraries

Conclusion

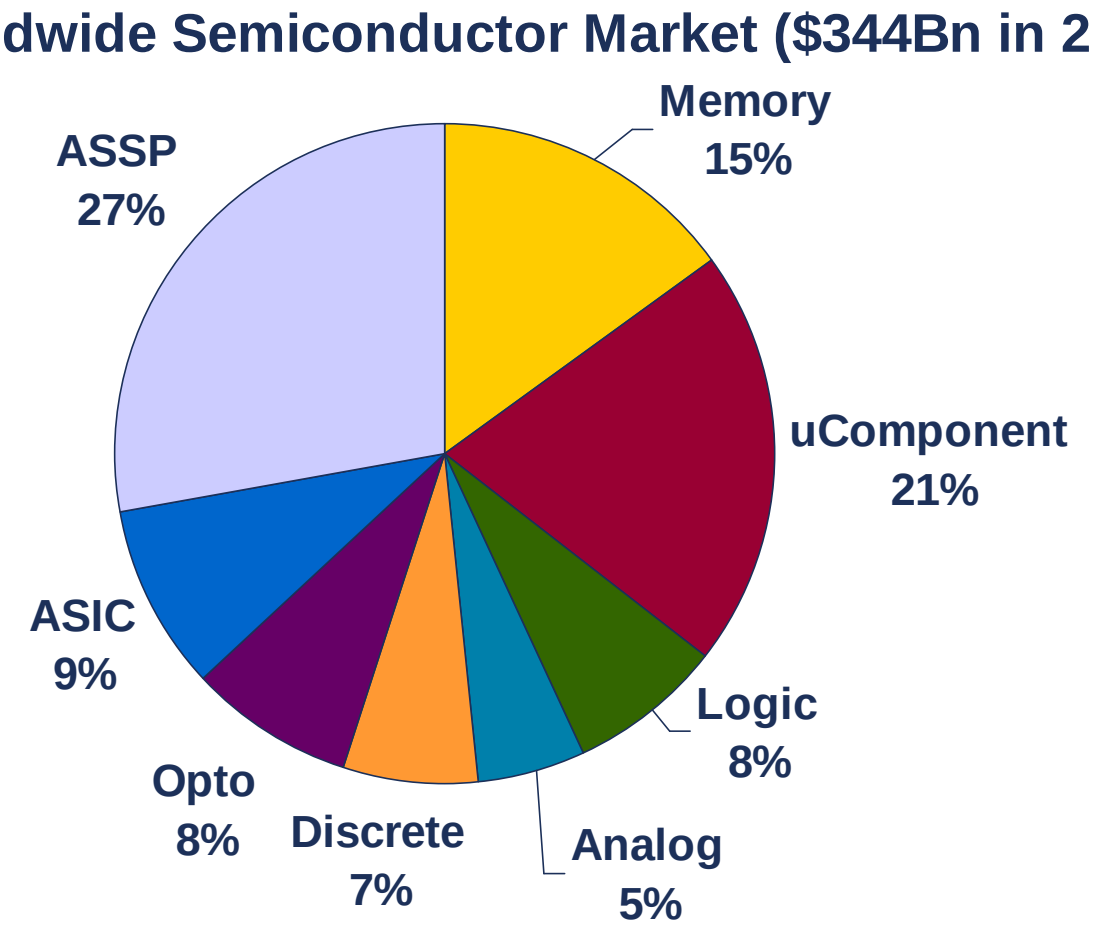
- Library development continues to get more complex
- Greater need for “know how”
  - IP content of libraries is increasing
- Greater need for compute infrastructure
  - Economies of scale can be achieved by outsourcing
- New techniques required to increase manufactured yield
  - Requires greater emphasis on R&D
- ARM will continue to evolve architectures to increase value
  - Ideally placed to benefit from tougher challenges

Market Opportunity for ARM Physical IP

Neal Carney

VP Marketing, PIPD

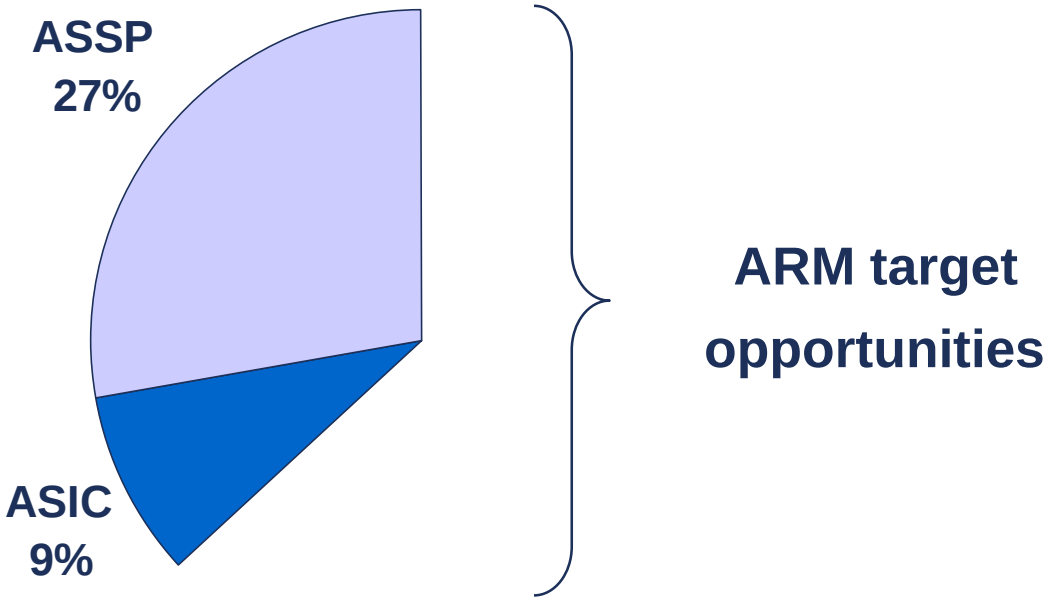
Semiconductor Industry Structure



Source: Gartner Q1 2006

Semiconductor Industry Structure

Worldwide Semiconductor Market ($344Bn in 2010)

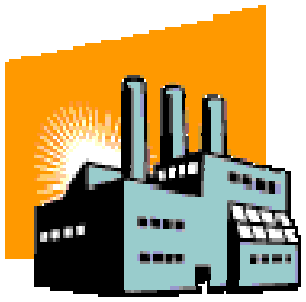


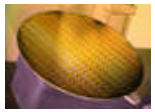
Source: Gartner Q1 2006

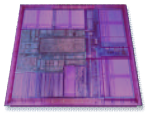
Industry Structure – ASIC and ASSP

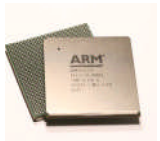
Foundry/Fabless Model

Foundry Company

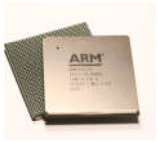








Fabless Semiconductor



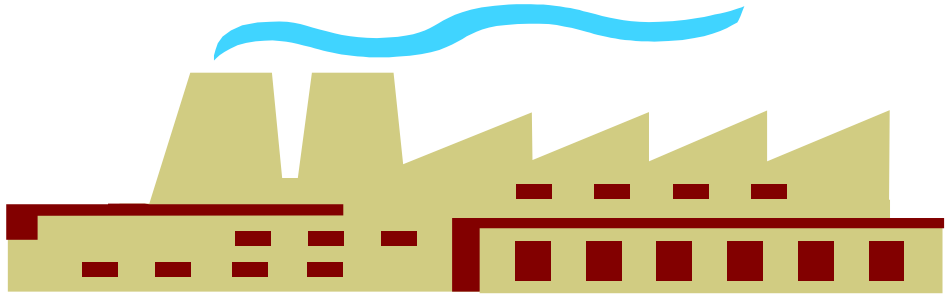
Value chain

IC Design

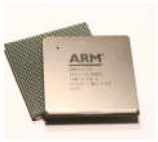
Wafer Fab → Test → Packaging → Sales and Distribution

IC Design

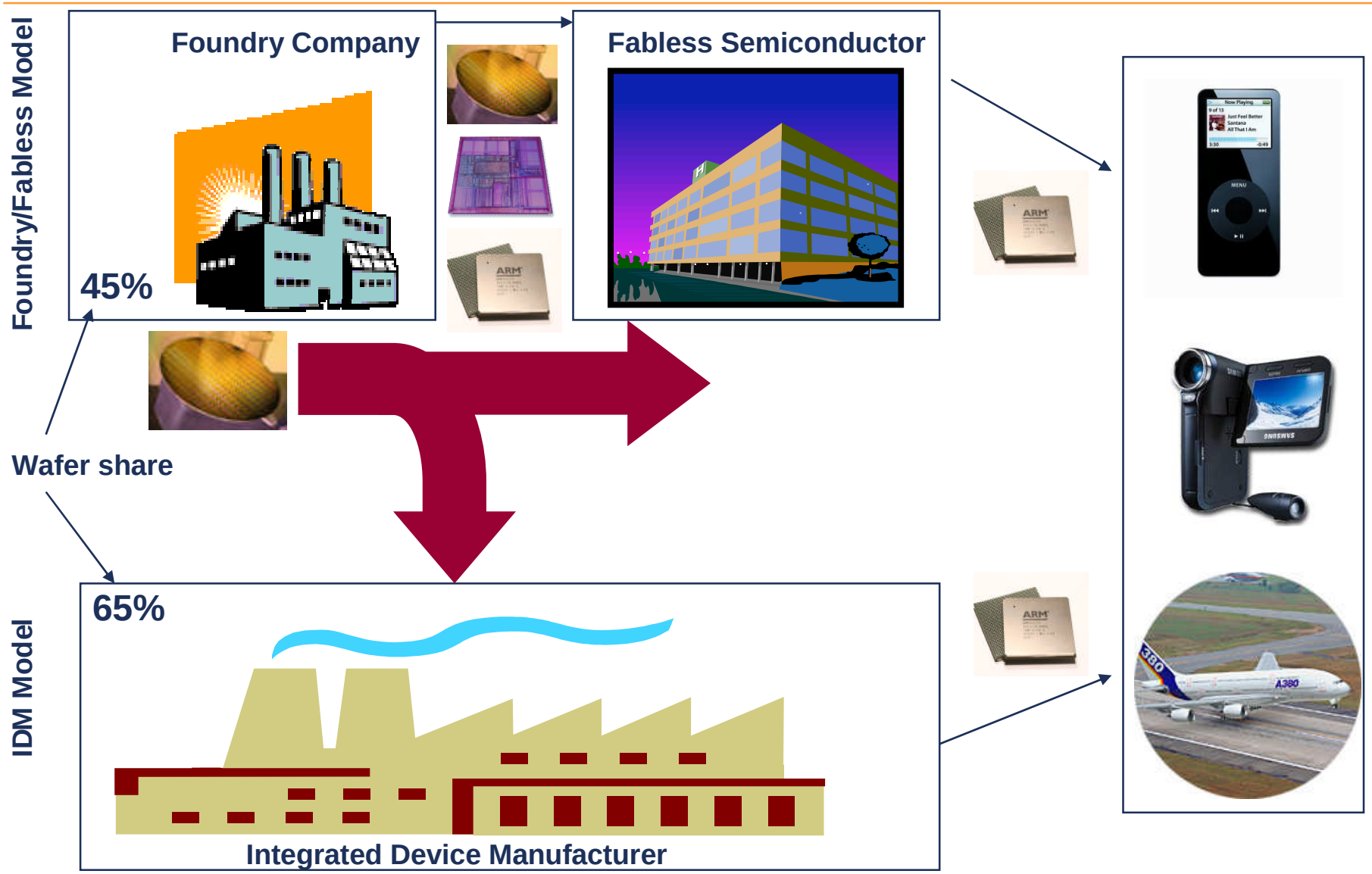
IDM Model



Integrated Device Manufacturer



Industry Structure – ASIC and ASSP



Leading Companies in ASIC/ASSP

Leading Foundries	2005
TSMC	$ 8,220
UMC	$ 2,822
SMIC	$ 1,171
Chartered	$ 1,132
IBM Microelectronics	$ 832
MagnaChip (Hynix	$ 396
Vanguard	$ 354
DongbuAnam	$ 347
HH NEC	$ 305
Jazz	$ 210

Leading Fabless	2005
Qualcomm	$ 3,457
Broadcom	$ 2,606
Nvidia	$ 2,203
Sony	$ 1,982
ATI	$ 1,736
Marvell	$ 1,712
Agere	$ 1,530
MediaTek	$ 1,438
Conexant	$ 813
RFMD	$ 691
Micronas	$ 533
VIA	$ 524
CSR	$ 486
Avago	$ 467
Bosch	$ 466

Leading IDM's	2005
TI	$ 6,889
ST	$ 4,581
Intel	$ 3,826
Philips	$ 3,810
Infineon	$ 2,679
IBM Microelectronics	$ 2,380
Toshiba	$ 2,239
Freescale	$ 2,209
NEC	$ 1,785
Renesas	$ 1,768
Fujitsu	$ 1,764
Matsushita	$ 1,415
LSI Logic	$ 1,244
Samsung	$ 1,031
Rohm	$ 973

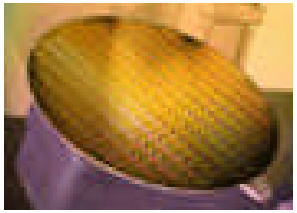
Source: Gartner Q1 2006

Positive Industry Trends for Physical IP

Semiconductor Factory Economics

$3 Billion
Capital Investment

Optimum Scale – 30K wafers/mo.



Annual wafer output – 360K

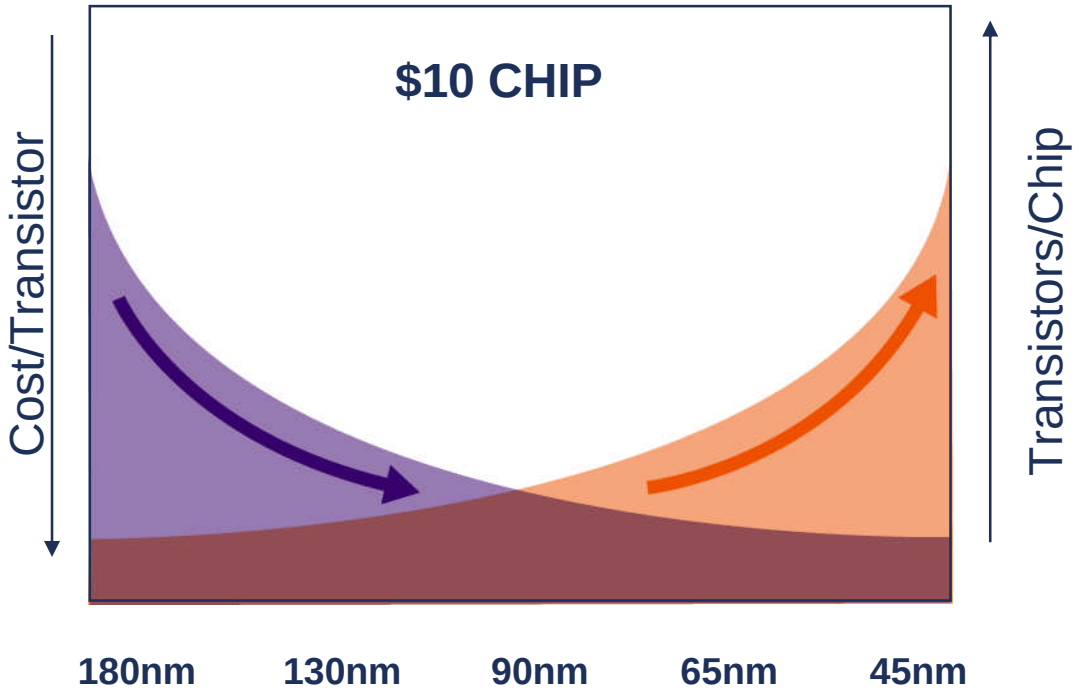
Average revenue per wafer - $3,000 - $5,000

Annual revenue required to "fill the fab" - $1.3bn to $1.8bn

- Conclusions:
  - Critical mass of customers required
  - Must compete in all segments – ASIC, ASSP and Foundry
  - Boundaries between ASIC, Foundries and IDMs blurring

Increasing Design Complexity

- More functionality, same or lower price
- Chip design, verification
- IP design and proliferation



- **Design complexity and costs increasing**
- **Economics drive alliances and outsourcing to lower design costs**
  - **IP reuse**
  - **Focus on value add**

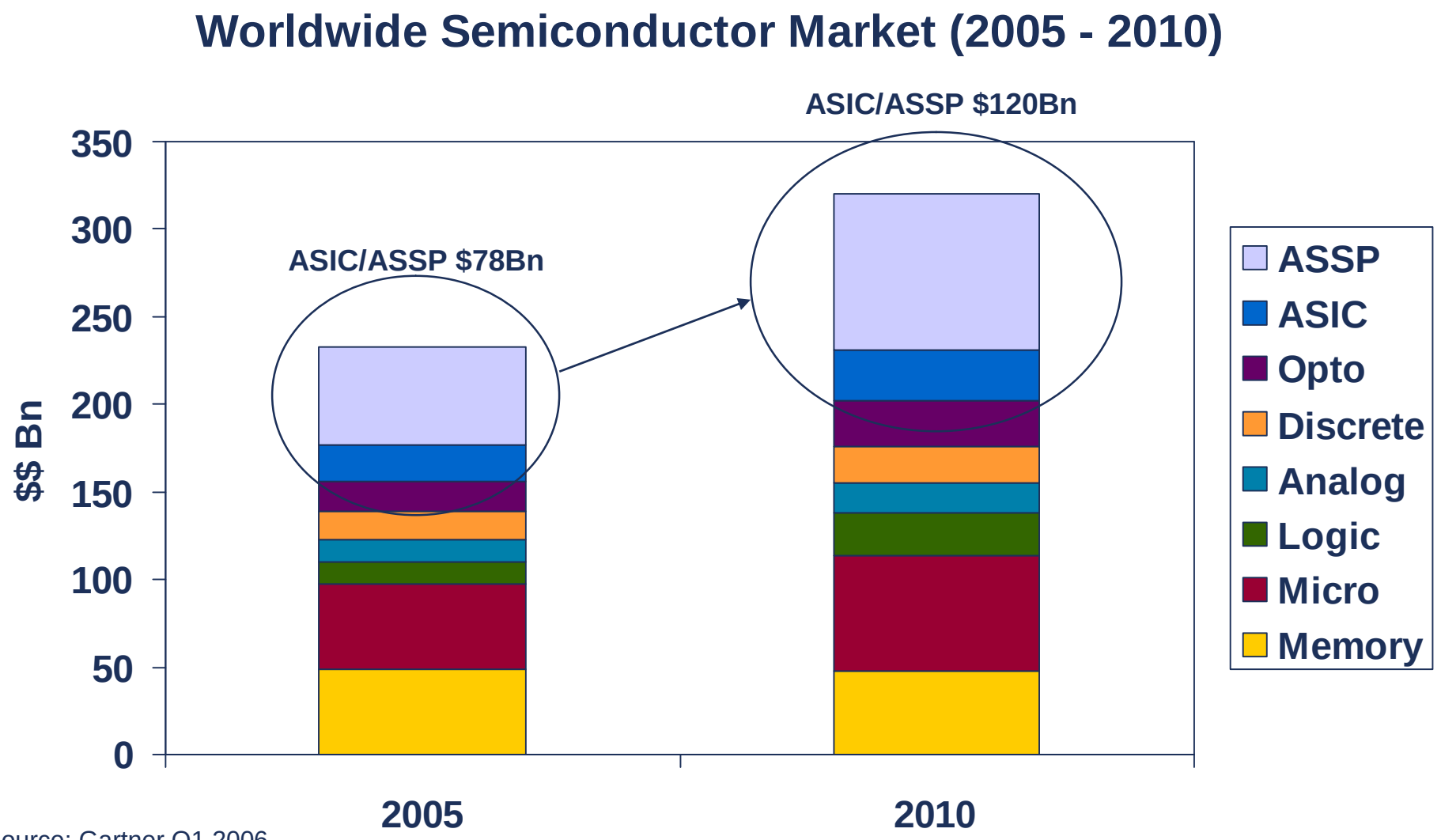
Positive Industry Trends for Physical IP

- Economics
  - Boundaries between ASIC, Foundries and IDMs blurring
    - New points of entry for Physical IP to increase share
  - Horizontal alliances and specialisation
    - IBM Common Platform (IBM, CHRT, Samsung, Infineon)
    - Crolles Alliance (ST, Philips, Freescale – TSMC process technology)

Positive Industry Trends for Physical IP

- Complexity
  - Outstripping IDM's ability do everything internally
    - Outsource activity with less differentiation – Libraries
  - Close coupling of system design with physical design
    - ARM processors co-developed with Physical IP
      - Processor + Physical Implementation
    - Superior solution from ARM
      - Performance, Power, Cost (Area*Yield)
      - Accuracy – Design matches actual silicon
    - Time-to-market advantage
      - Processor and physical implementation delivered simultaneously

Opportunity for Physical IP

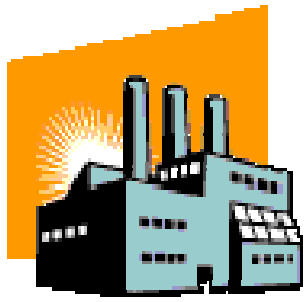


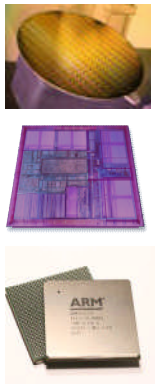
Source: Gartner Q1 2006

ASIC/ASSP Value Chain (Wafer vs. Chip)

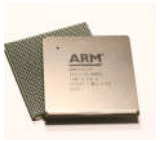
Foundry/Fabless Model

Foundry Company





Fabless Semiconductor



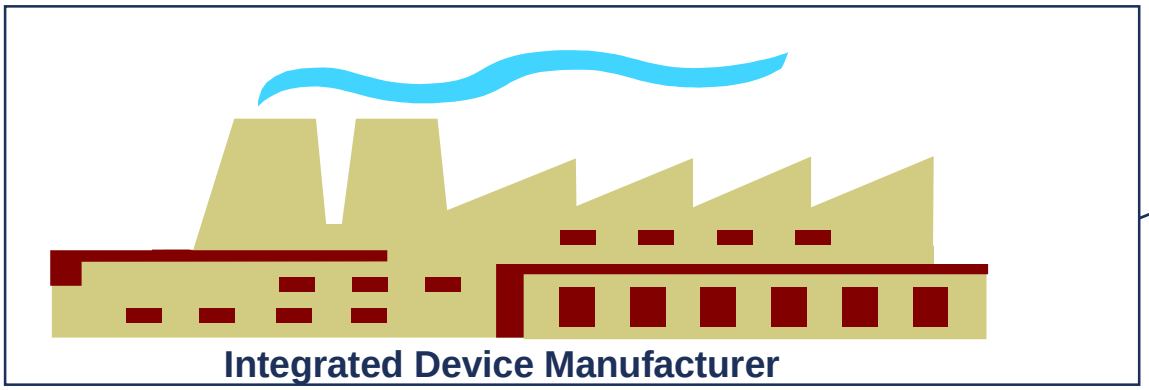
Value chain

$4.00 + $2.00 = $6.00 + $4.00 = $10.00

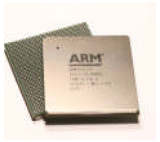
(Margin)

Wafer Fab → Test → Packaging → Sales and Distribution

IDM Model



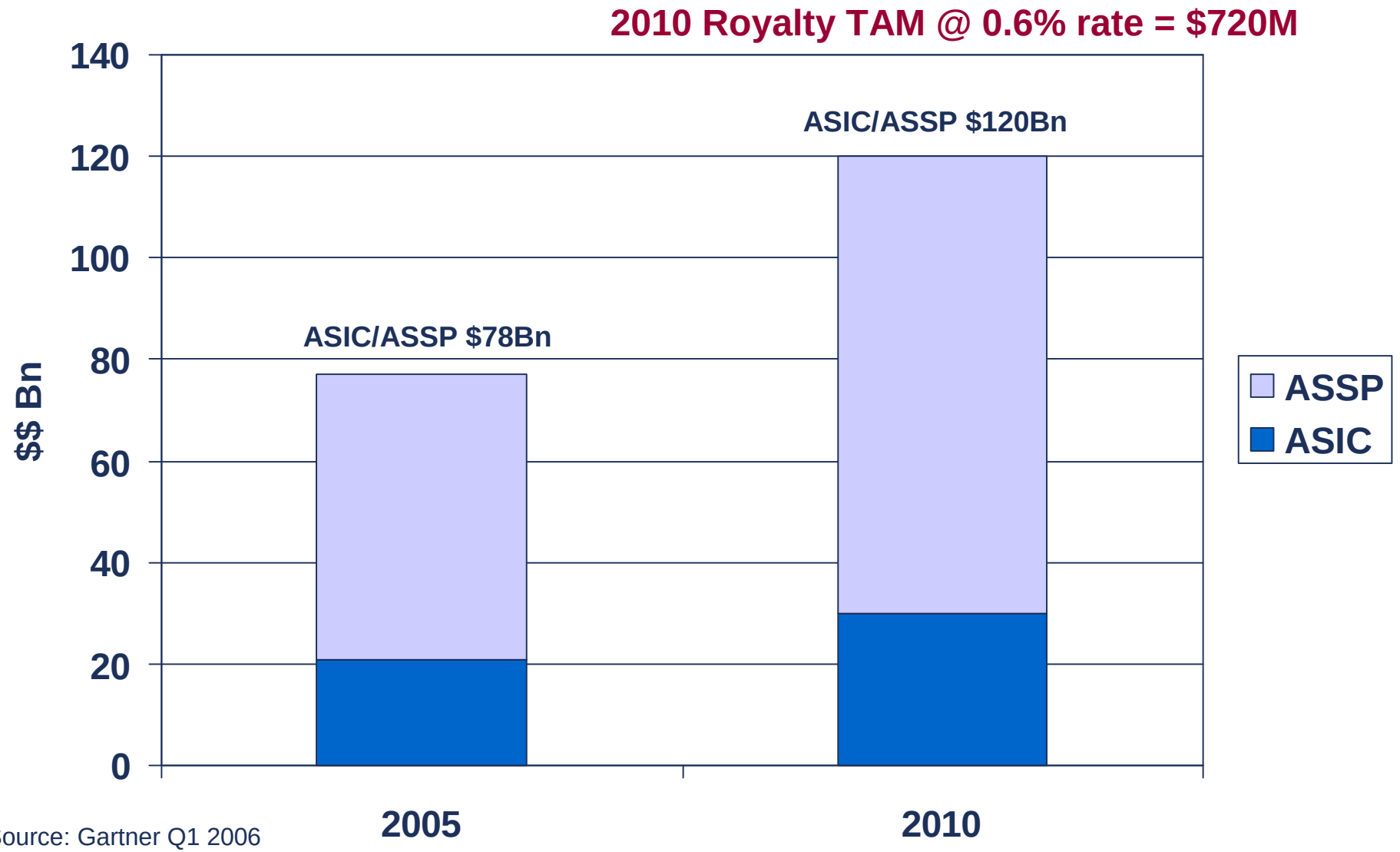
Integrated Device Manufacturer



Opportunity for Physical IP

- Royalty Total Available Market in 2010 = $720M
  - Assumes 0.6% PIPD net royalty at the chip level of value
  - Reference – $0.06 on a $10 chip
- 0.6% Royalty on chip ~ 1.5% net royalty on a wafer
  - Wafer value is ~ 40% of chip value (2.5x multiplier-wafer to chip)
  - PIPD business model includes a royalty credit-back program
    - Gross royalty paid by foundry set aside for use as portion of future license fee
- 0.6% of chip value is consistent with royalty rates we obtain from foundries today
  - Conservative rate for 2010
  - ARM will be adding additional physical IP content
    - PHYs currently add 0.5-1.0%
    - Additional memory types

PIPD Total Available Market



Source: Gartner Q1 2006

PIPD Scorecard

Leading Foundries	2005
TSMC	$ 8,220
UMC	$ 2,822
SMIC	$ 1,171
Chartered	$ 1,132
IBM Microelectronics	$ 832
MagnaChip (Hynix	$ 396
Vanguard	$ 354
DongbuAnam	$ 347
HH NEC	$ 305
Jazz	$ 210

Leading Fabless	2005
Qualcomm	$ 3,457
Broadcom	$ 2,606
Nvidia	$ 2,203
Sony	$ 1,982
ATI	$ 1,736
Marvell	$ 1,712
Agere	$ 1,530
MediaTek	$ 1,438
Conexant	$ 813
RFMD	$ 691
Micronas	$ 533
VIA	$ 524
CSR	$ 486
Avago	$ 467
Bosch	$ 466

Leading IDM's	2005
TI	$ 6,889
ST	$ 4,581
Intel	$ 3,826
Philips	$ 3,810
Infineon	$ 2,679
IBM Microelectronics	$ 2,380
Toshiba	$ 2,239
Freescale	$ 2,209
NEC	$ 1,785
Renesas	$ 1,768
Fujitsu	$ 1,764
Matsushita	$ 1,415
LSI Logic	$ 1,244
Samsung	$ 1,031
Rohm	$ 973

Blue shading indicates public use of ARM Physical IP

Source: Gartner Q1 2006

Conclusions

- Royalties key to attractiveness of the Physical IP business
- Significant royalty market is available to ARM
  - Industry trends lowering barriers to external physical IP in IDMs
  - Technology trends favoring wider adoption of ARM physical IP
- Key to success is driving market share of leading Foundry, ASIC and ASSP companies
- Good progress to date
  - TSMC multi-generation library deal
  - Adoption by IBM ASIC
  - Samsung foundry and ASIC using ARM libraries

Coffee Break

Financial Models for ARM Physical IP

John McAdoo

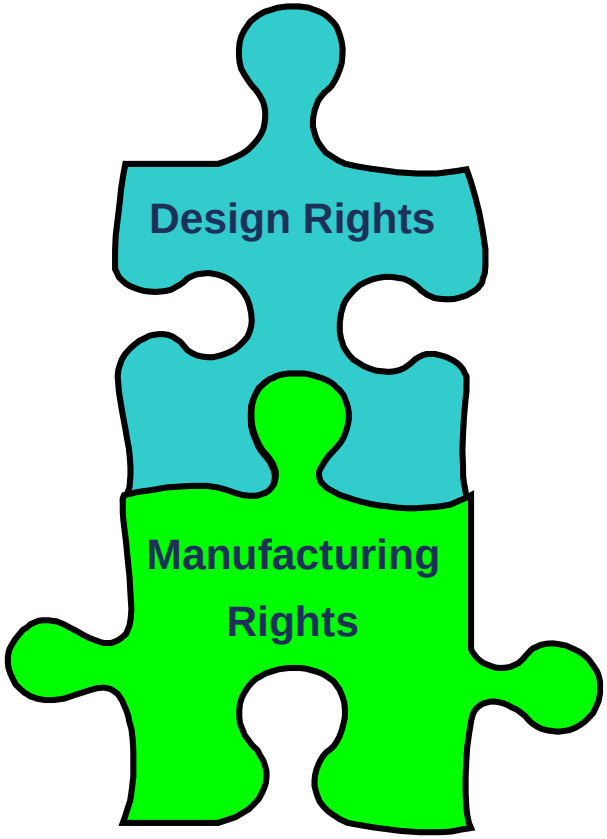
VP Finance, PIPD

Agenda

- PD and PIPD licensing models
  - PIPD license types
- PIPD foundry license opportunity
  - PIPD license data Q1 2006
- Revenue recognition process
- PIPD royalty process
- Conclusions

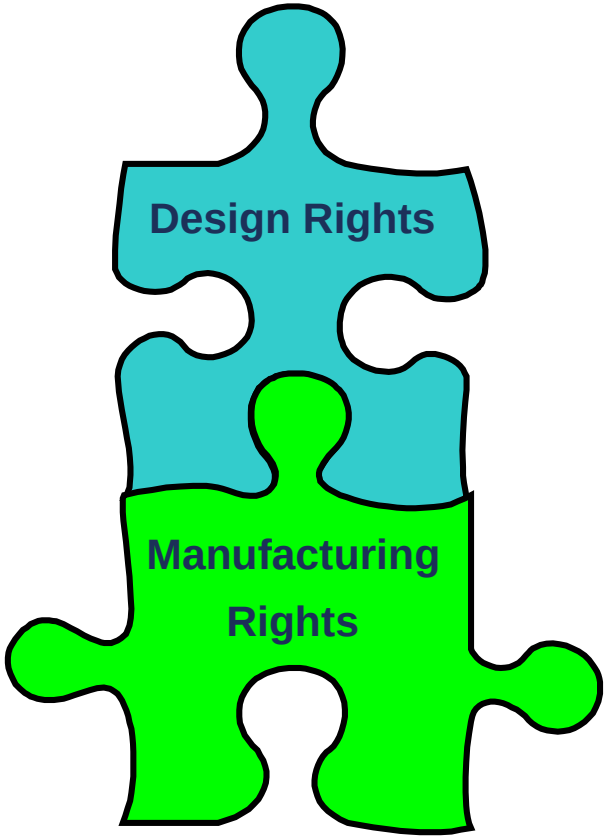
Semiconductor IP Licensing Model

- All Semiconductor IP licenses contain 2 parts
  - Design rights
  - Manufacturing rights
- Differ on license term and extent of rights granted
- Processor Division
  - Design and manufacturing rights grouped into one license
  - Foundry Program
    - Design rights are sold to fabless chip designer for license fee and royalty
    - Manufacturing rights are sold to foundry for license fee



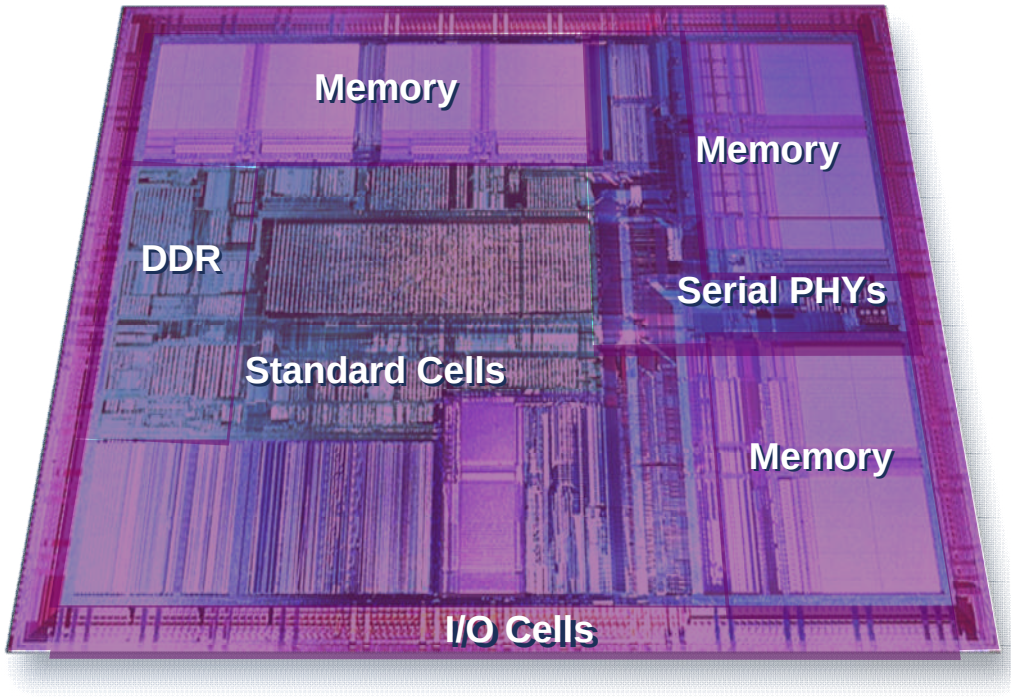
Physical IP Follows the Same Model

- Foundry - Free Library Program
  - Design rights free to the chip designer
  - Manufacturing rights sold to the foundry for license fee and royalty
- Foundry - End User License
  - Design rights and ‘have’ manufactured rights sold to the chip designer for license fee
  - Associated manufacturing rights already granted to relevant foundry (foundry pays royalty)
- IDM license
  - Design and manufacturing rights sold to an IDM for license fee and royalty



Physical IP Products

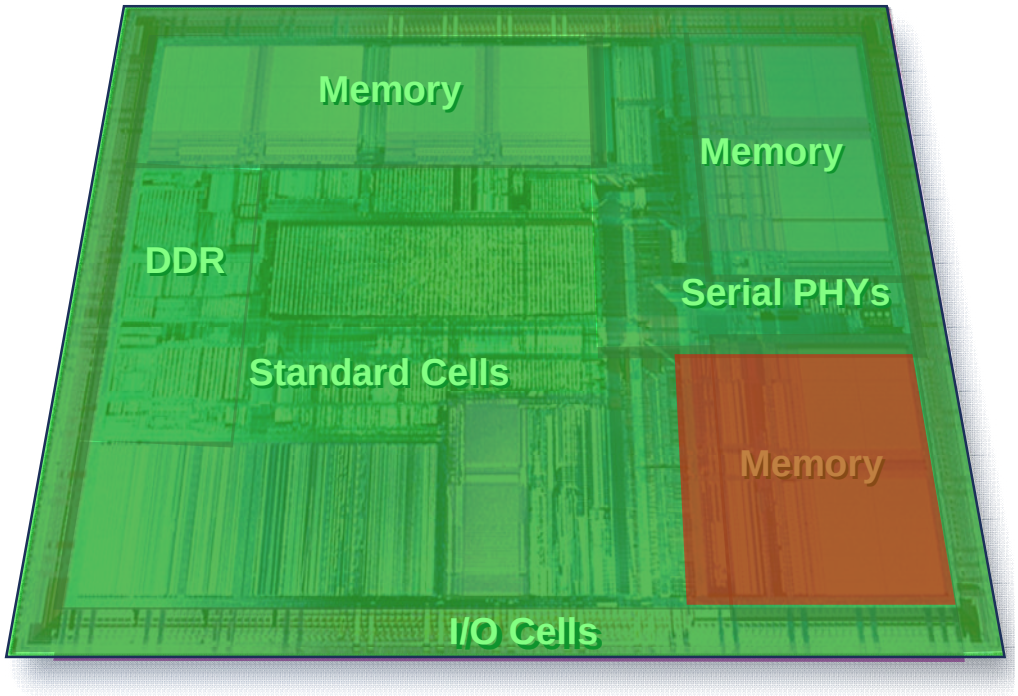
- Library platforms
  - Standard cells
  - Embedded memory
  - I/O functionality
- High-speed interfaces
  - DDR
  - Serial PHYs



Physical IP Products and Licenses

Platform License

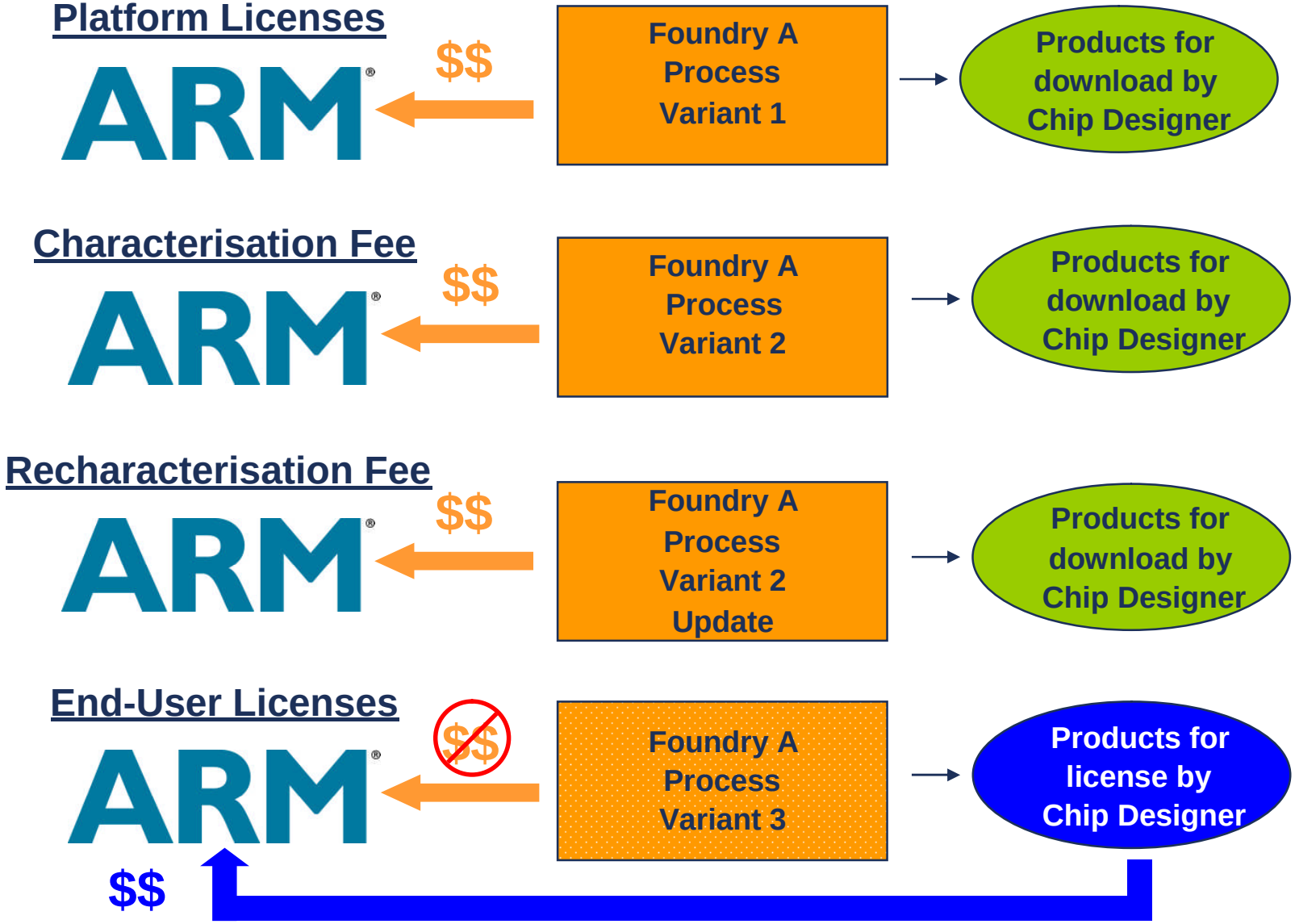
- Customer: Foundries and IDMs
- Contains a number of components (example:1 cell library, 5 memory compilers)
- Perpetual, multi-use license
- Typical license fee: $1M-$3M



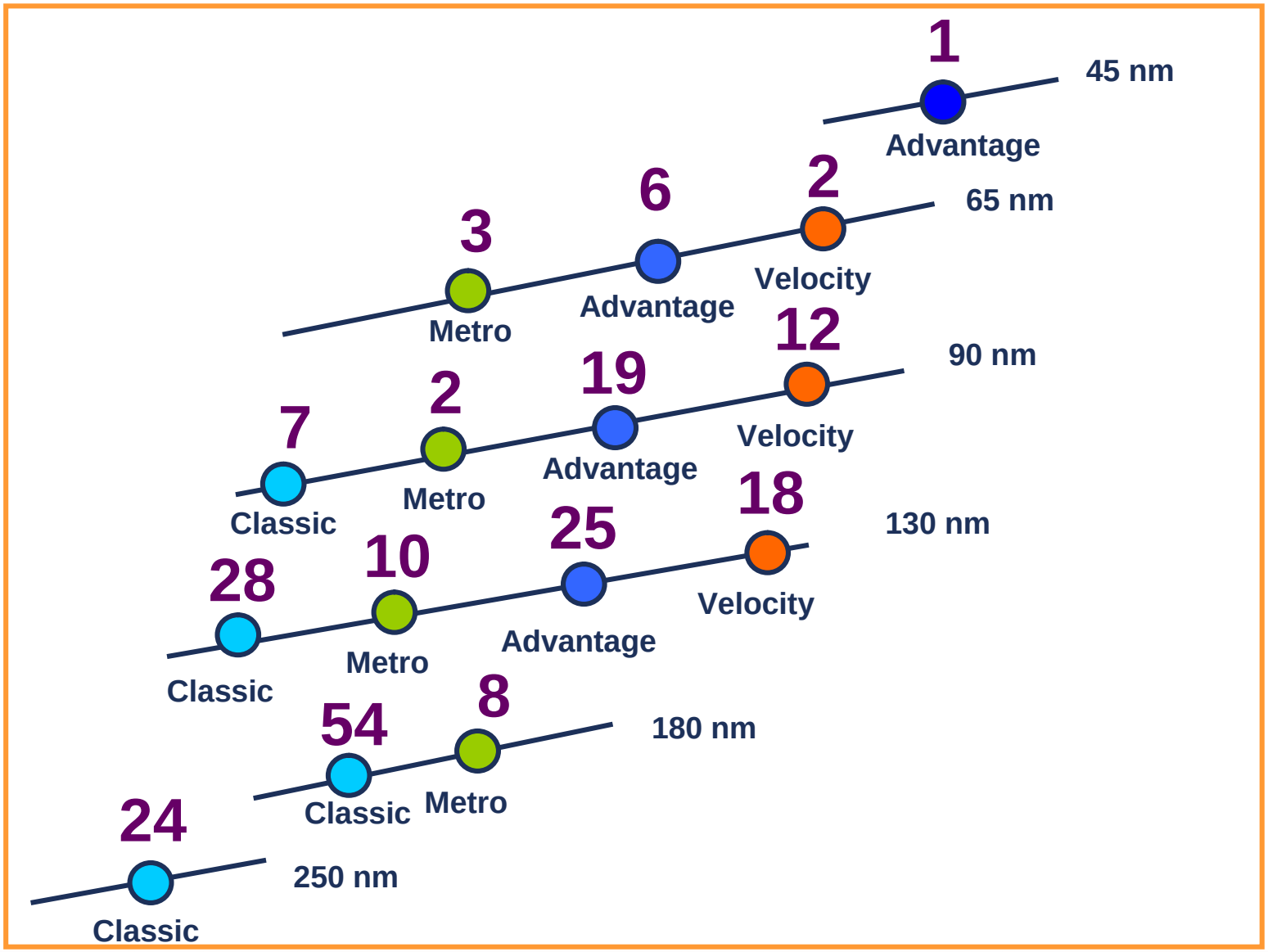
End-User License

- Customers: IDMs and fabless semiconductor companies
- Contains a single component
- Per-use and multi-use licenses
- Typical license fee: $50K-500K

PIPD Foundry License Opportunity



PIPD Licensing – Cumulative Q1 06



PIPD Revenue Recognition

- Engineering effort is managed to balance:
  - Near-term customer requirements (customisation activity)
  - Long-term new product developments (R&D activity)
- Revenue recognised on % of completion (POC) method
- Newer technologies are extending recognition period
  - Conversion period now approximately 3-4 quarters
- Health of the business is measured by bookings
  - Equates to revenue + backlog
- Backlog will eventually turn into revenue

Revenue Recognition Example

- Product is 80% complete when license is signed

- 25% of the remaining customisation work is completed by quarter end

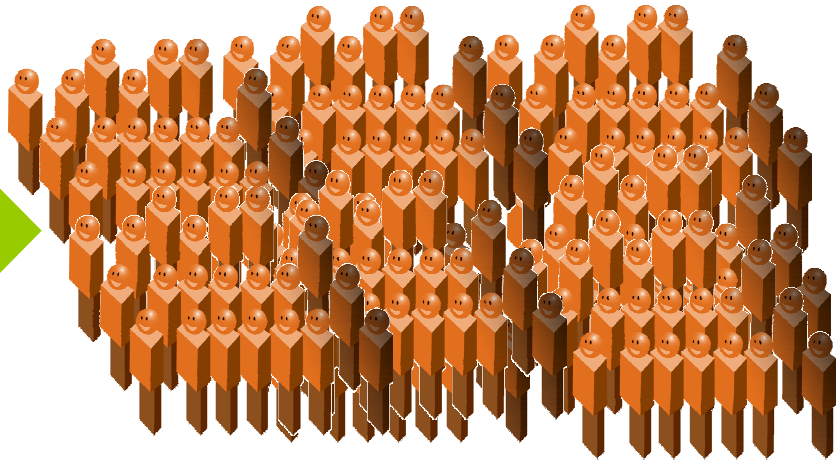
Royalty Process

Chip Designer:

Downloads IP for free from ARM

Sends design to Foundry

Sends part information to ARM



THE CHALLENGE:

1000s of chip designers

1000s of part numbers

Immature systems

ARM®

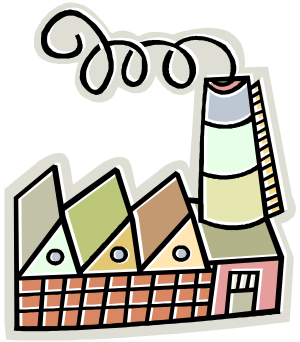
Foundry:

Licenses IP from ARM

Sends wafers to the chip designer

Sends part information to ARM

Sends royalties to ARM



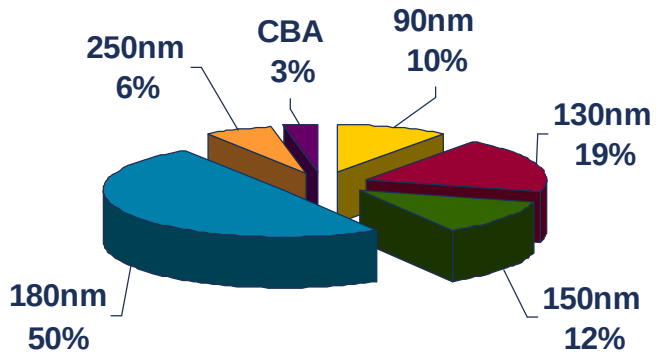
Royalty Catch-up

- Historically Artisan relied predominately on third-party audit
- ARM investing internally in data analysis and royalty tracking processes to improve visibility
  - Supplemented by third-party independent audits
- Areas of focus:
  - Complete, accurate and timely reporting
  - Data reconciliation between end users and foundry
  - Investigation of differences between users and foundries
- Investment in internal processes yielding benefits
  - Improved royalty tracking systems in place
  - Catch-up royalty being identified internally
- Opportunity for further improvement
  - Better royalty visibility over time

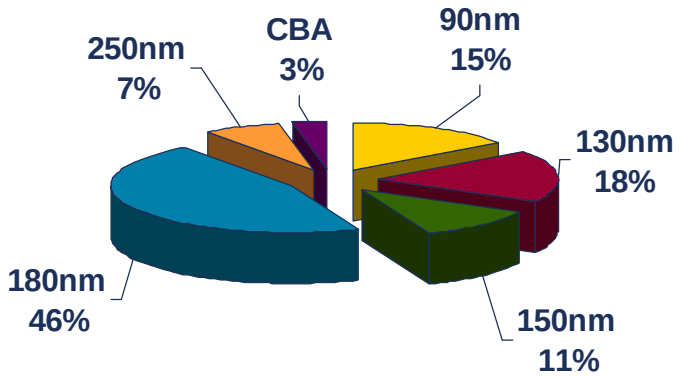
Royalty Analysis by Process Node

- Internal data analysis enabling more trend analysis
- 90nm technologies are fastest growing contributor
- Older process nodes still contributing over 50%
- Nodes have significant longevity

Q4 2005



Q1 2006



CBA = Cannot be attributed

Summary

- PD and PIPD licensing models are similar
- Opportunity for increased licensing
  - More foundries taking ARM Physical IP
  - Extended matrix of process variants and PIPD product types
- Royalties being earned across process nodes
  - Demonstrates longevity of physical IP
  - Function of cumulative licensing
  - Growth being led by newer technologies
- Royalty visibility improving
  - Increased investment in infrastructure and data analysis

Summary

- Economics of IP outsourcing apply to multiple technologies at different times
- Silicon complexity increases the market opportunity and competitive position of ARM's Physical IP business
- Current market position and outsourcing opportunity drives significant PIPD royalty upside
- Microcontrollers represent a significant emerging volume opportunity for ARM – we have assembled the right products and tools to win
- Timelines for semiconductor IP are long – returns can be very large
- ARM is executing well and has a bright future