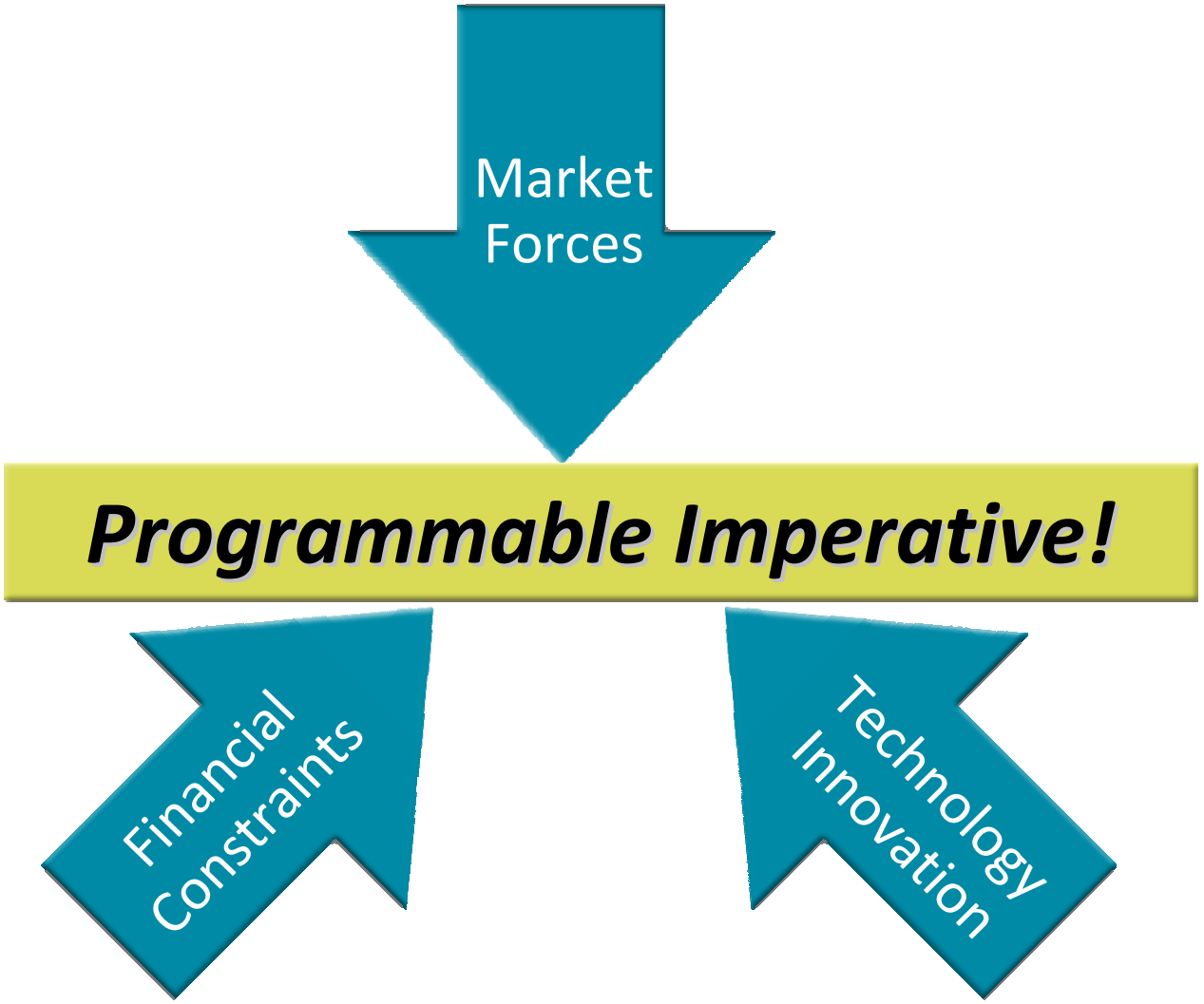
The Programmable Imperative: Reaching the Tipping Point

Moshe Gavrielov,
President and CEO

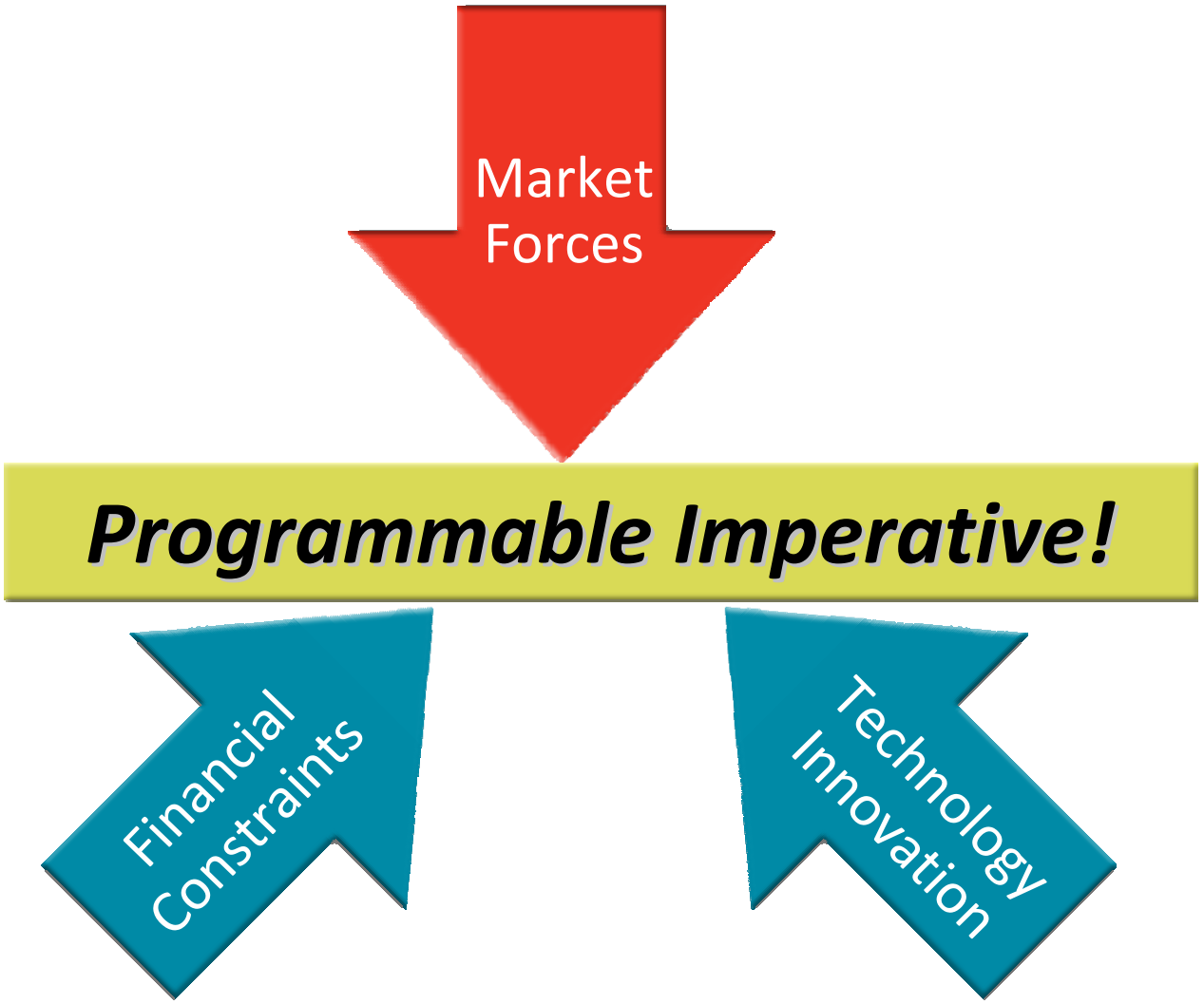
Safe Harbor Disclaimer

During the course of this presentation, we may provide projections or other forward-looking statements regarding future events and/or future financial performance. We wish to caution you that such statements are just predictions and that actual events or results may differ materially. We refer you to the documents the Company files from time to time with the Securities and Exchange Commission. Specifically, we refer you to the Company's last filed Forms 10-K and/or 10-Q. These documents contain and identify important factors that could cause the actual results to differ materially from those contained in our projections and other forward-looking statements.

The Time for Programmables is Now!



Market Forces



Key Market Trends

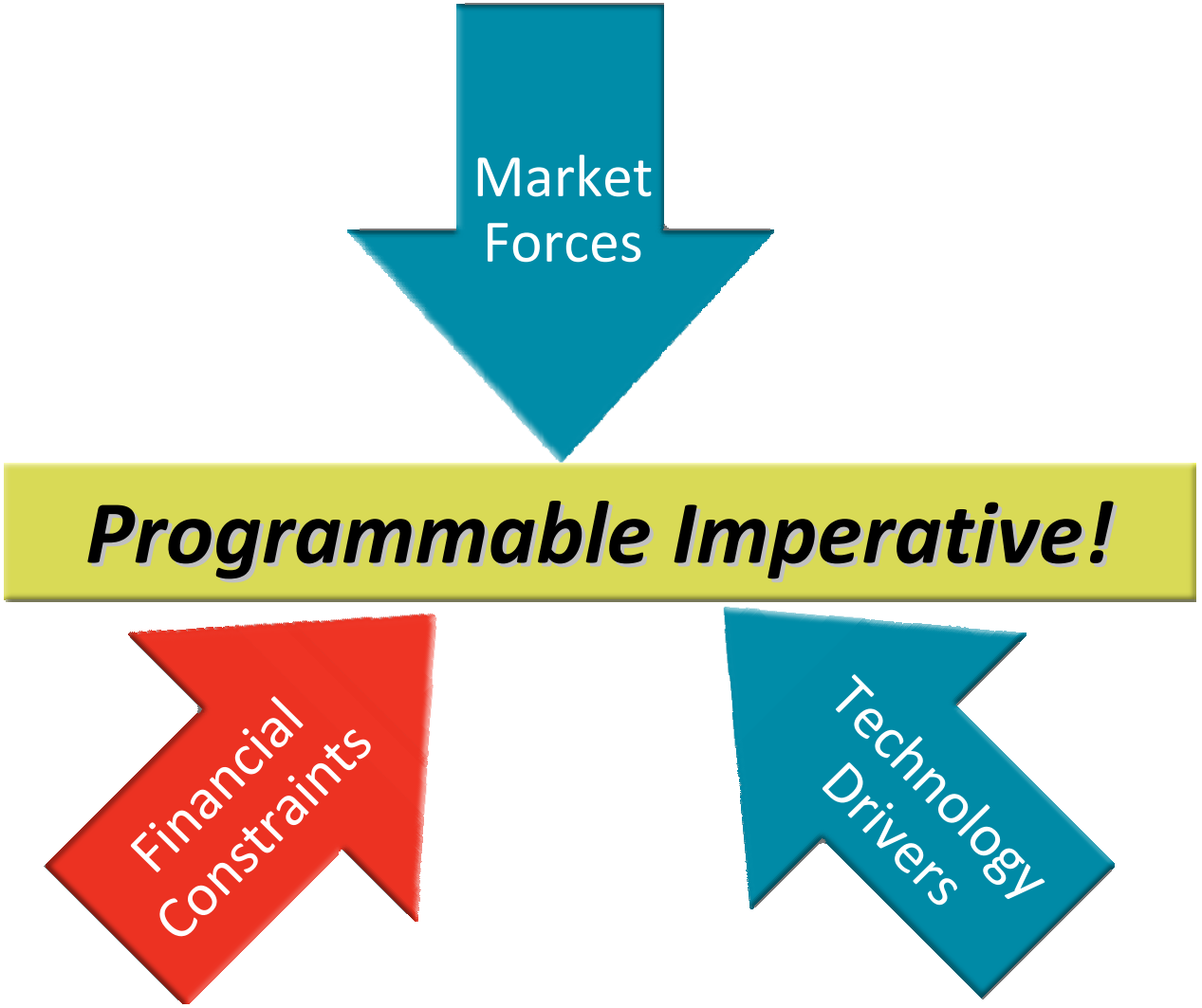
Rapid consumer-driven change

Hyper-connectivity

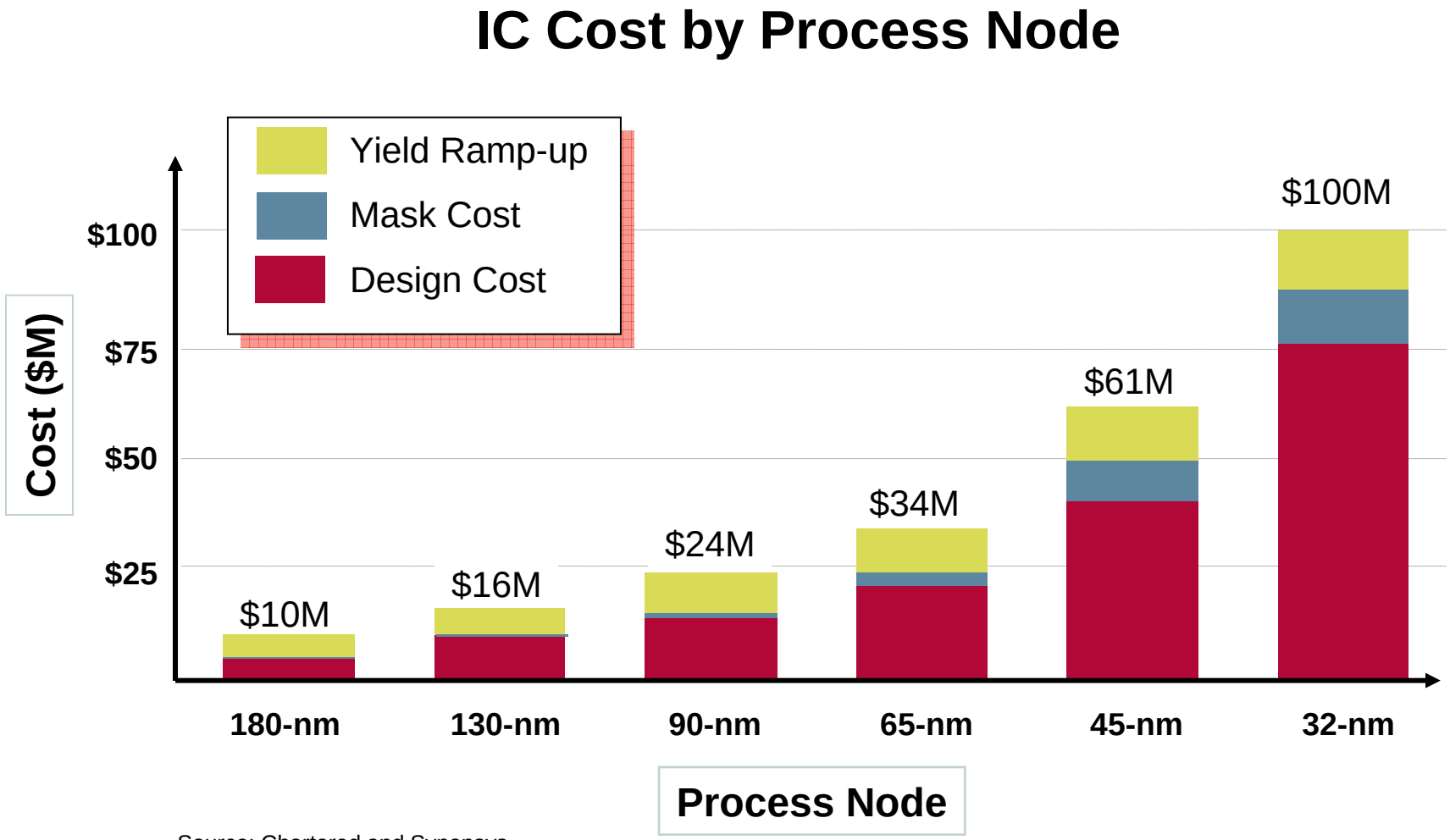
Fickle, fragmented markets

Time-to-market and flexibility: Key attributes for success

Financial Constraints



Rising ASIC/ASSP Development Cost Trend



Source: Chartered and Synopsys

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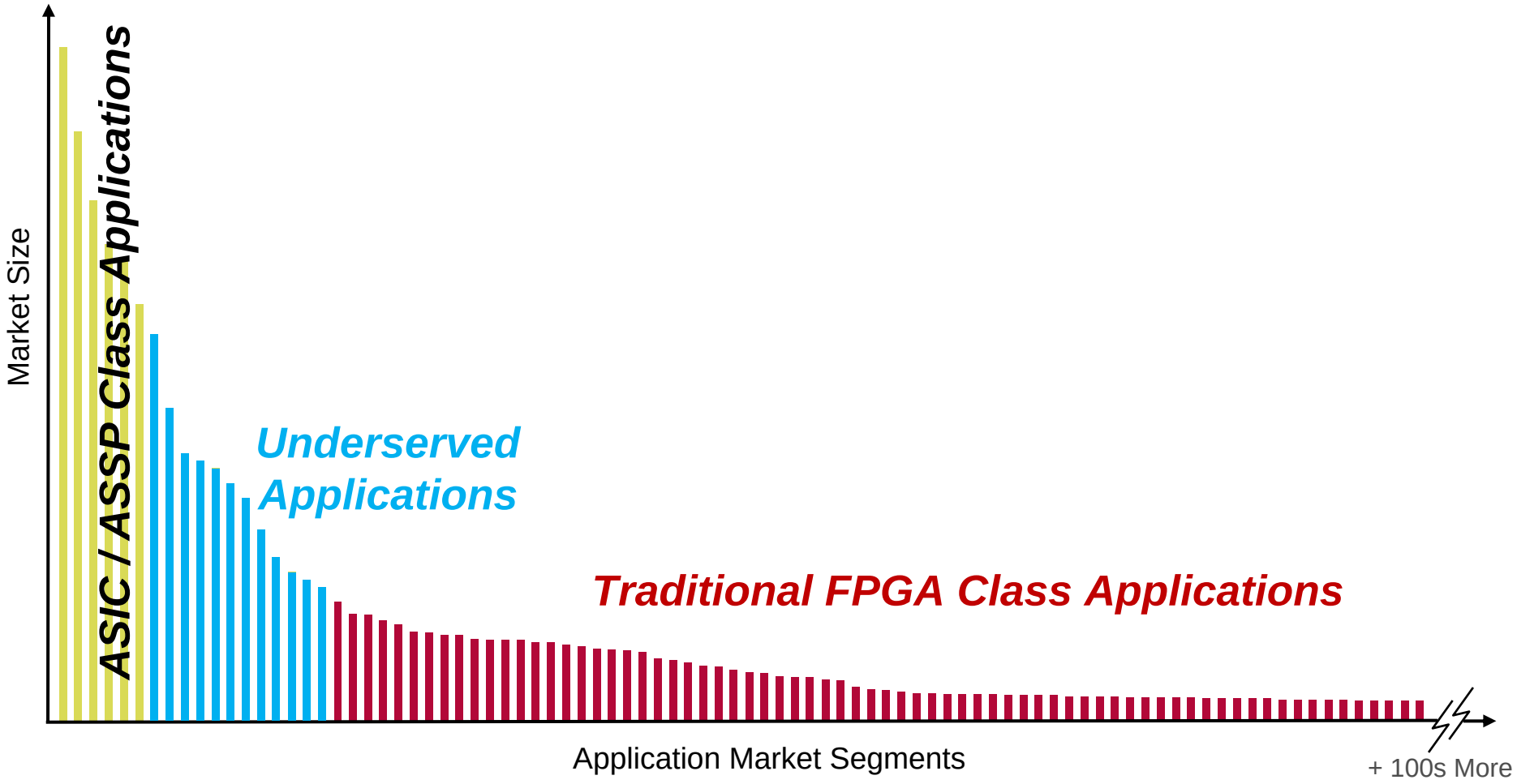
The Growing ASIC/ASSP Application Gap



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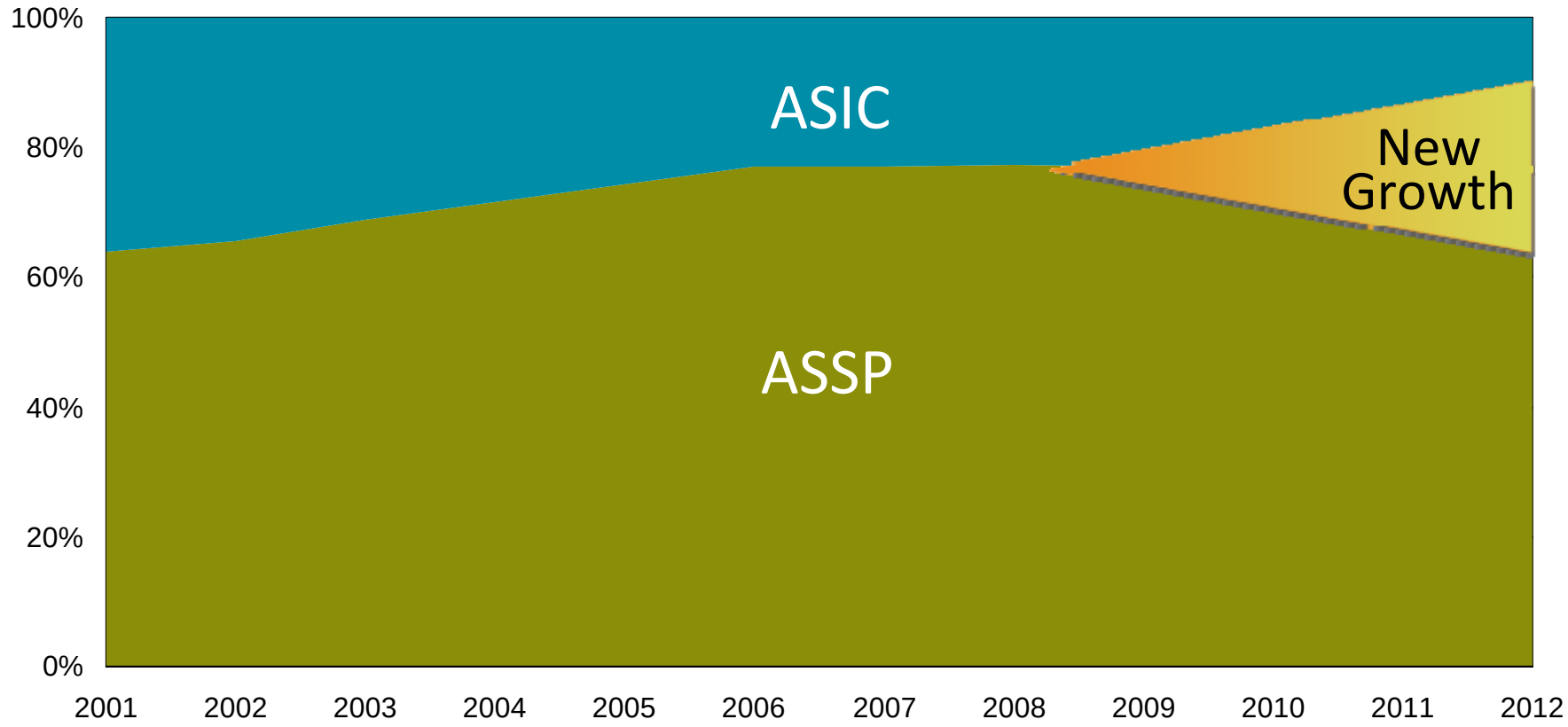
Xilinx Growth Opportunity Ahead



Source: iSuppli, March 2008

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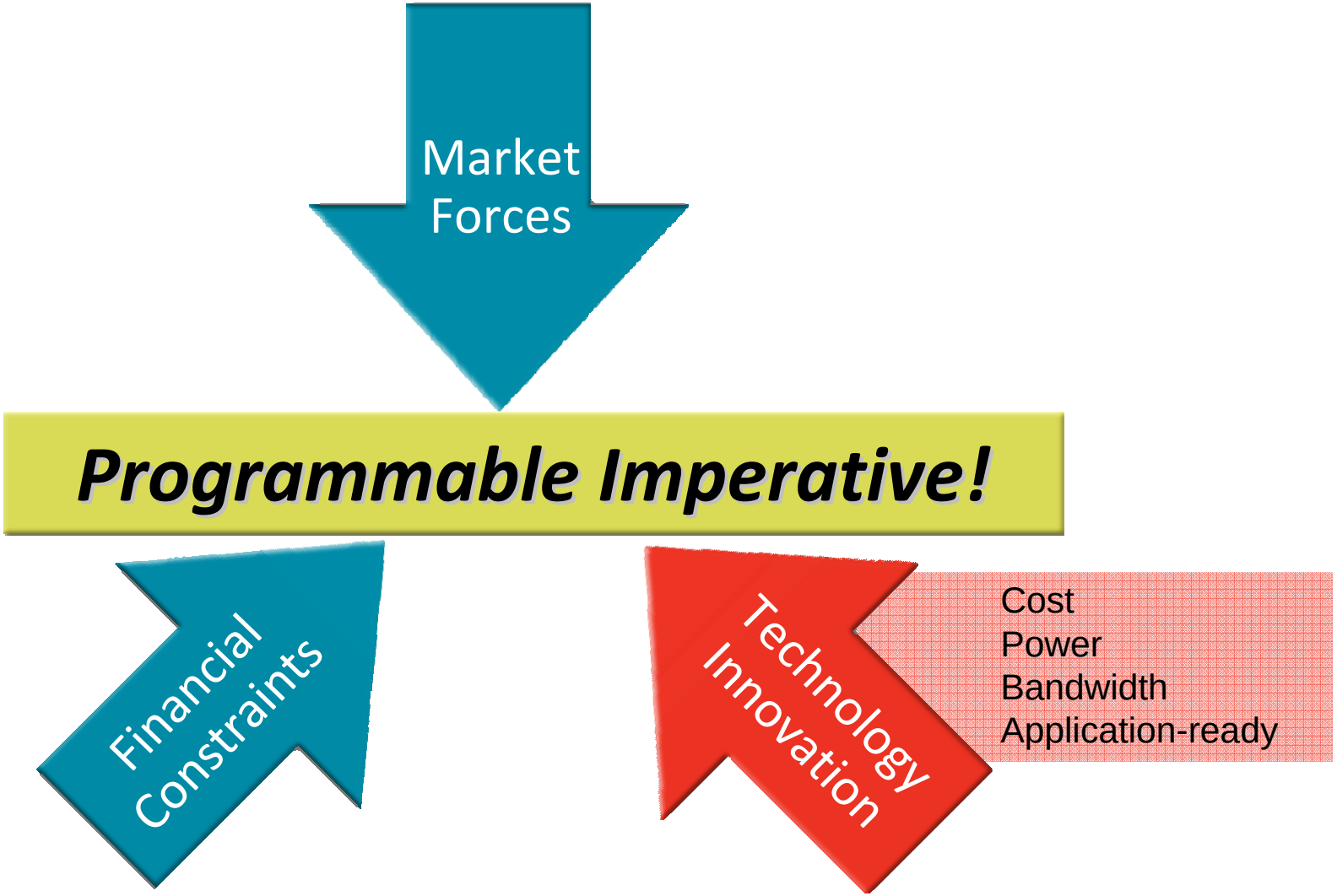
What it Means to our Customers

Do more with less	Improve engineering productivity
Reduce risk profile	Avoid big bets on ASIC design starts
Focus on core competencies	Differentiate or die

FPGA Technology Innovation



Introducing Virtex-6 and Spartan-6 FPGA Families

Deliver up to ***60%*** lower system cost

Cut power consumption by ***65%***

Reduce development time by ***50%***

Achieve over ***1Tbps*** IO bandwidth

Delivering customer breakthrough performance, power and cost benefits to push programmability beyond the tipping point

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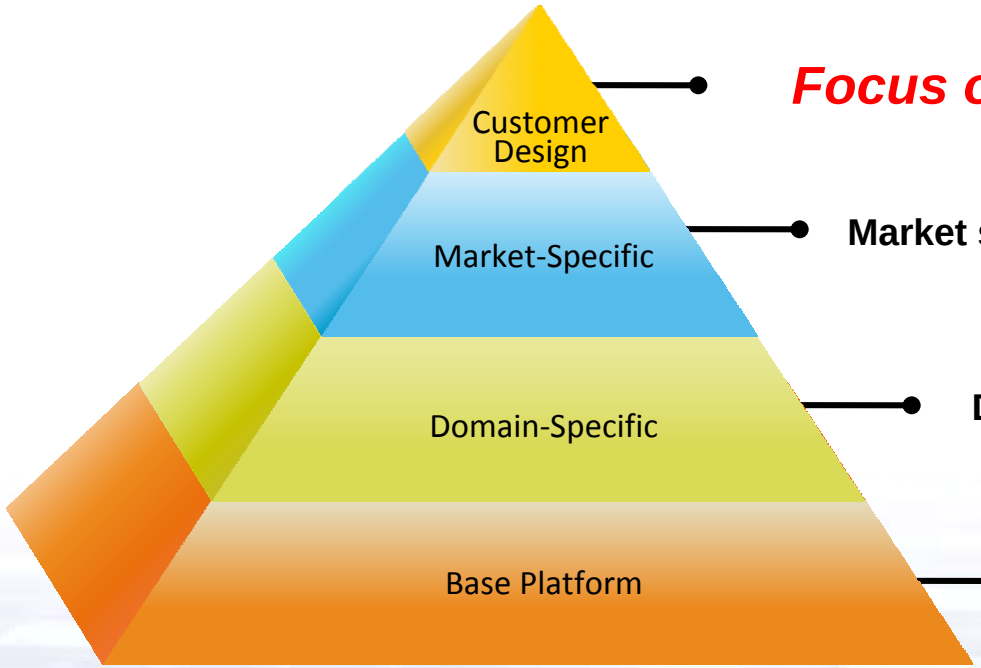
Targeted Design Platforms

Enabling customers to do more, faster…



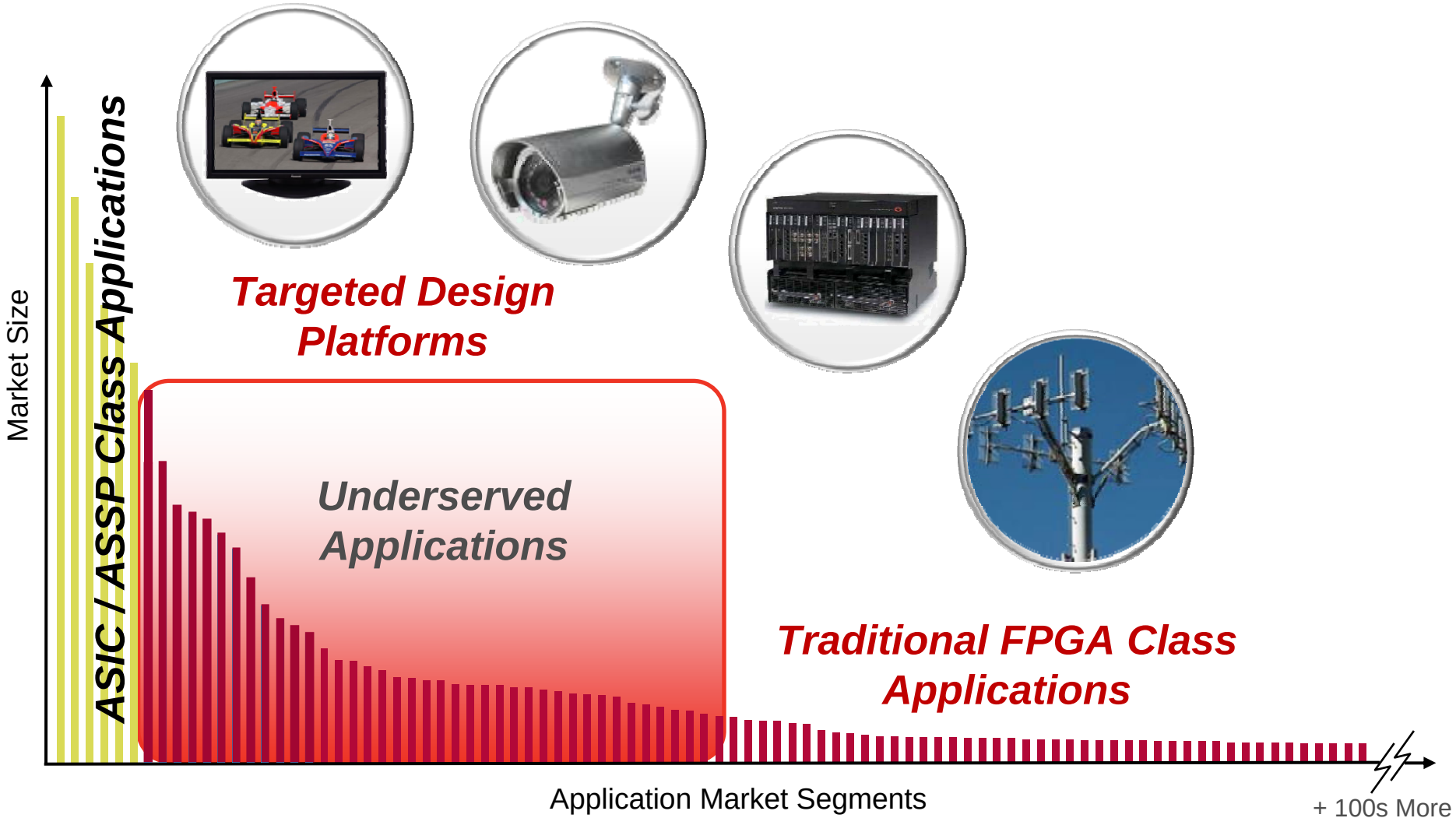
Focus on Differentiation

Communication • Video • AVB
Market specific IP, custom tools, custom boards

Embedded • DSP • Connectivity
Domain IP, Domain tools, FMC daughter cards

Virtex • Spartan
Base IP, ISE Design Suite, base boards

Targeted Design Platforms Broaden the Range of FPGA Applications



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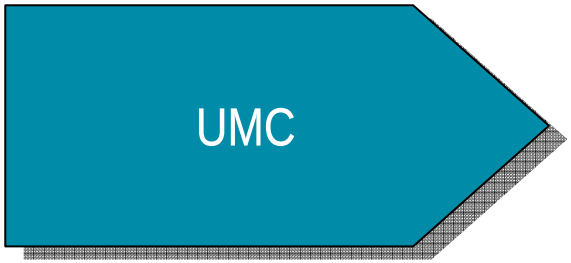
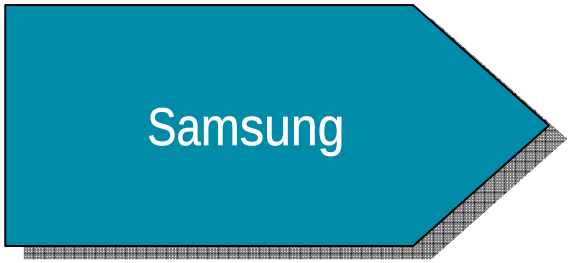
Next Generation Foundry Partners



Successful long term foundry partnership spans over one decade

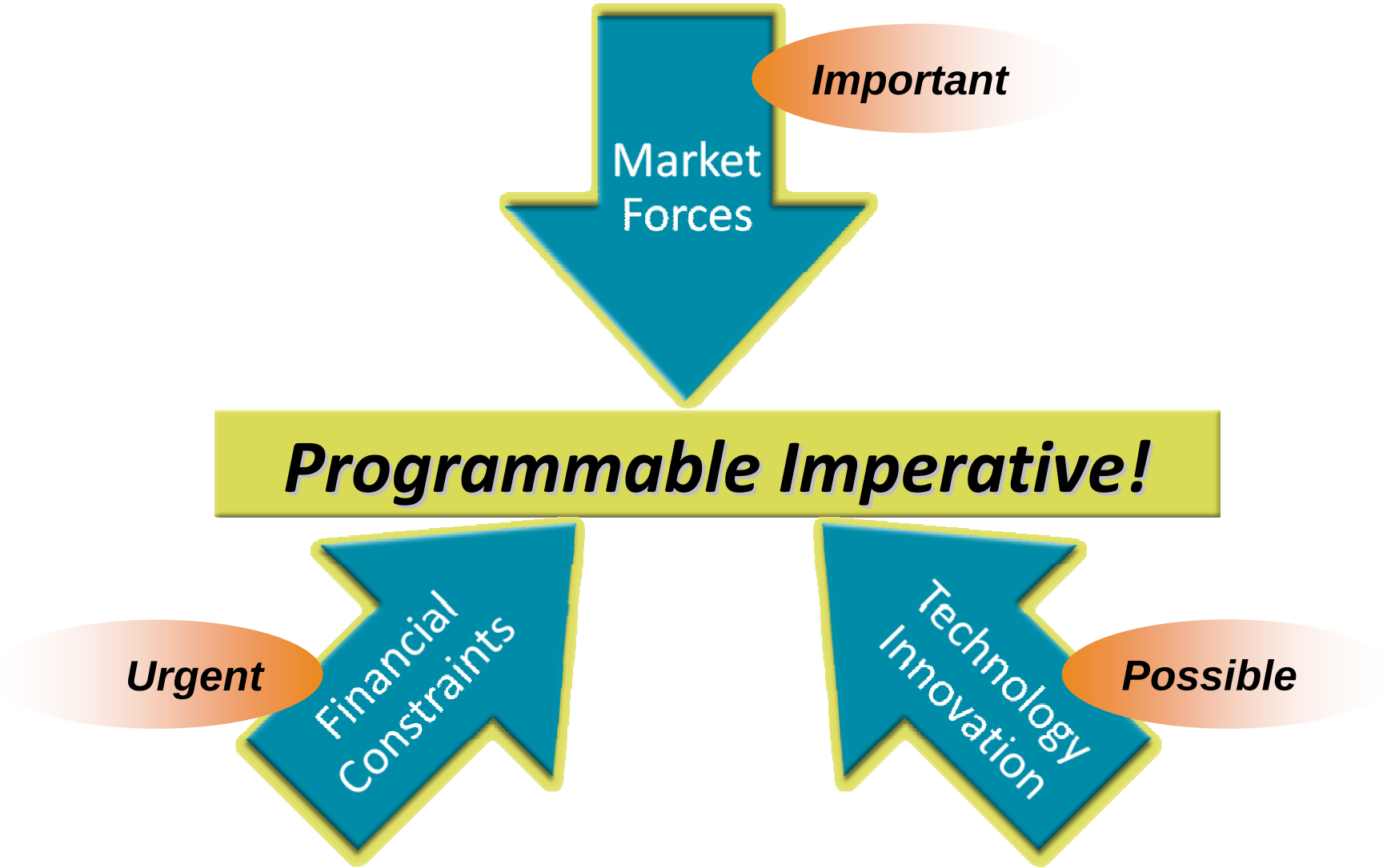


Proven high volume, low power, low cost manufacturer of advanced processes

Continued Commitment to Driving Product Development Efficiencies

- Centralized R&D and marketing organizations
- Parallel product release
- IP designed to be used across both architectures
- Leveraging industry IP & connection standards
- Driving additional R&D efficiency in next generation product development

The Time for Programmables is Now!



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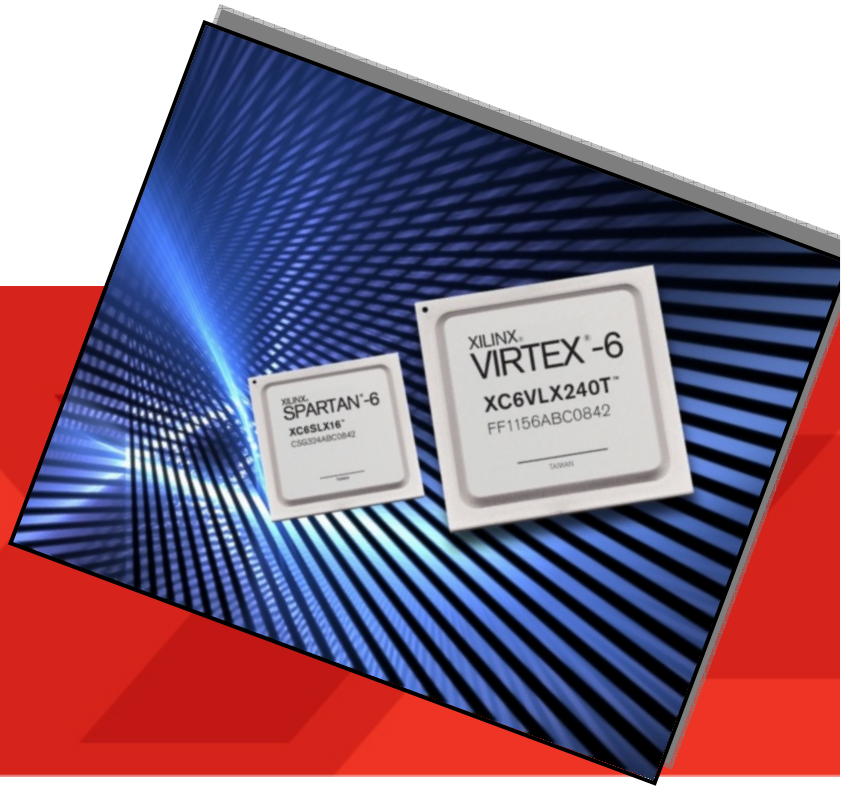
Introducing the Programmable Foundation for the Targeted Design Platforms

http://www.xilinx.com/6



Mustafa Veziroglu
Vice President, Product and Solutions Management

2-Feb-2009

Key Growth Opportunities for Xilinx

Increase picture quality of flat-panel displays

Drive next generation automotive infotainment

Improve security through real-time image interpretation

Enable “green” wireless base stations

Satisfy bandwidth demand in the wired infrastructure

Deploy a common, secure communication platform

Deliver flexible, dynamic, high resolution video and audio

Market Size

Application Market Segments

+ 100s More

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Virtex-6 and Spartan-6 FPGAs

Virtex-6 LXT
7 Devices

- High Density, High Performance
- Low-Power, 6.5 Gbps Serial Connectivity

Virtex-6 SXT
2 Devices

- High Density, High Performance
- Low-Power, 6.5 Gbps Serial Connectivity
- High Performance DSP Optimized

Virtex-6 HXT
2 Devices

- High Density, High Performance
- Ultra-High Performance 11.2 Gbps Serial Connectivity

Spartan-6 LX
7 devices

- Lowest Cost Logic

Spartan-6 LXT
4 devices

- Lowest Cost Logic
- Low Cost, Low Power 3.2 Gbps Serial Connectivity

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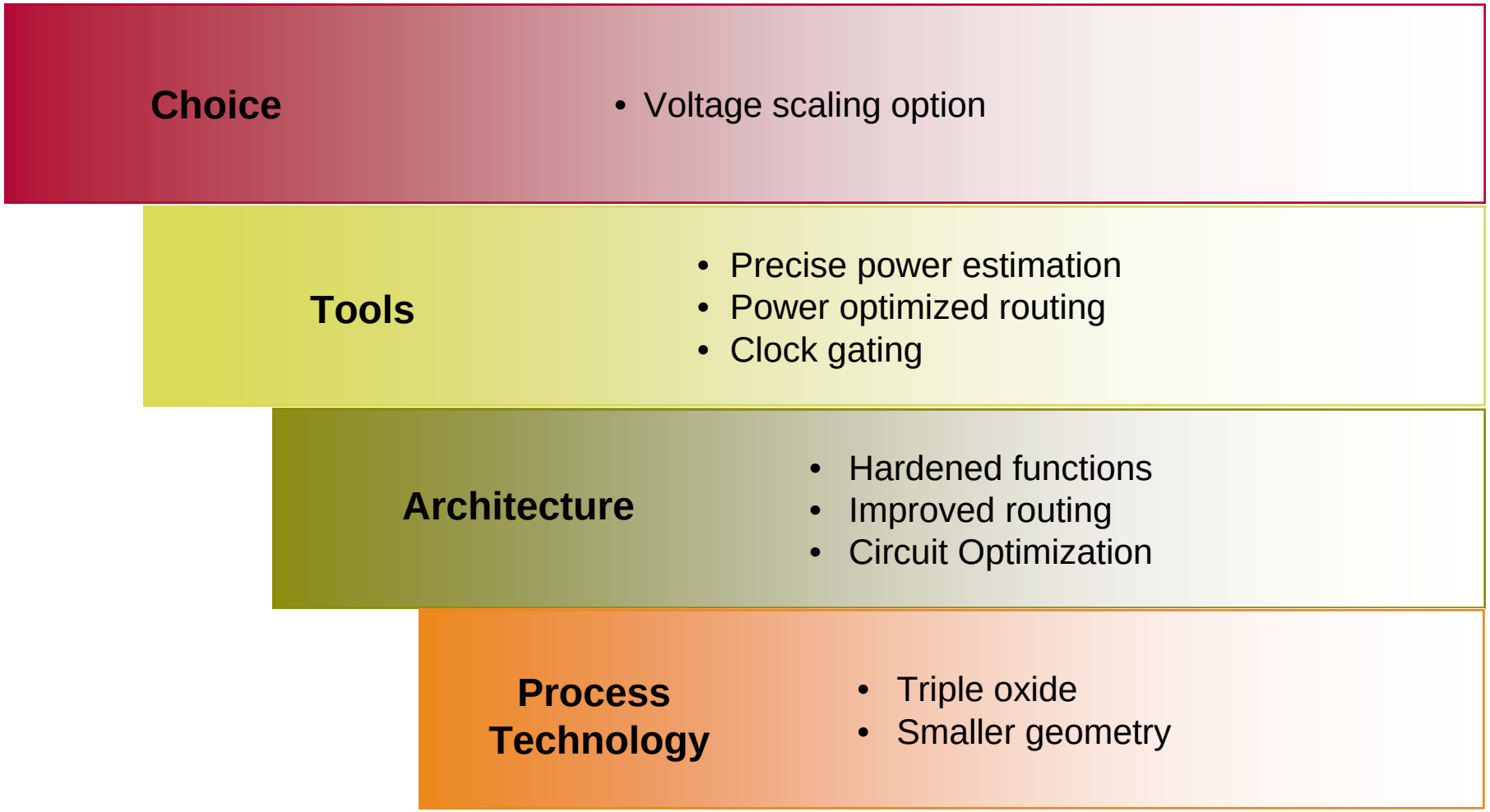
Low-Power by Design
Guiding Principle for TDPs



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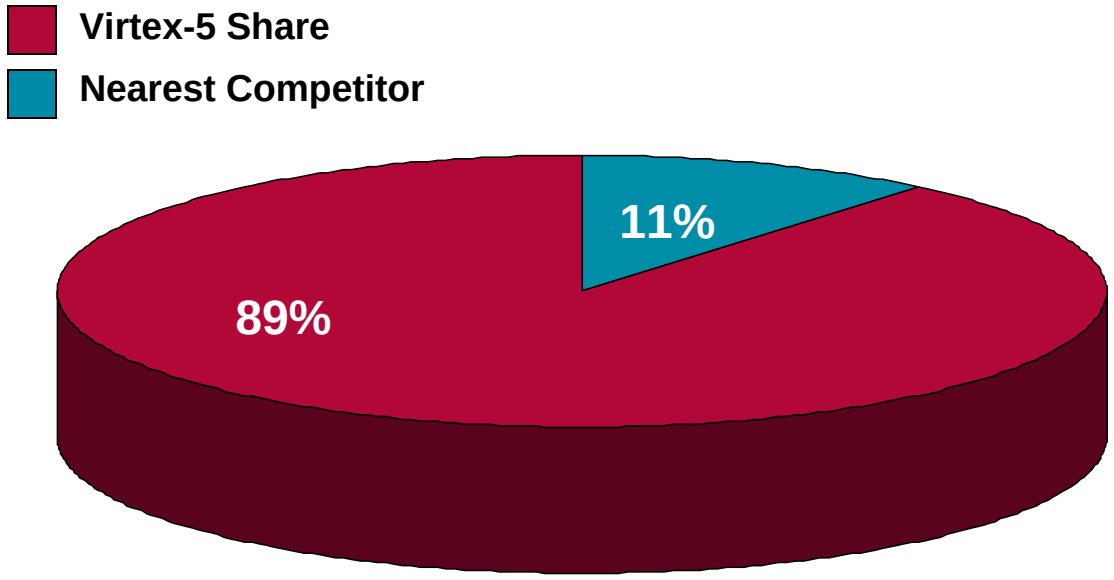
Building on Virtex-5 Market Leadership
High-end PLD market share – 4Q CY08 Sales



Over 7x Lead in Revenue vs. Nearest Competitor

Source: Xilinx Estimates, Company Reports

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Virtex-6 FPGAs Key Take Aways

- Lowest power, highest density, highest performance FPGA family
- Based on advanced 40nm, 12-layer metal process
- Three families, 11 devices
- 200+ early customer engagements
- Early access software support available today
- Samples in 2Q CY09, production in 4Q CY09
- Rapid family deployment

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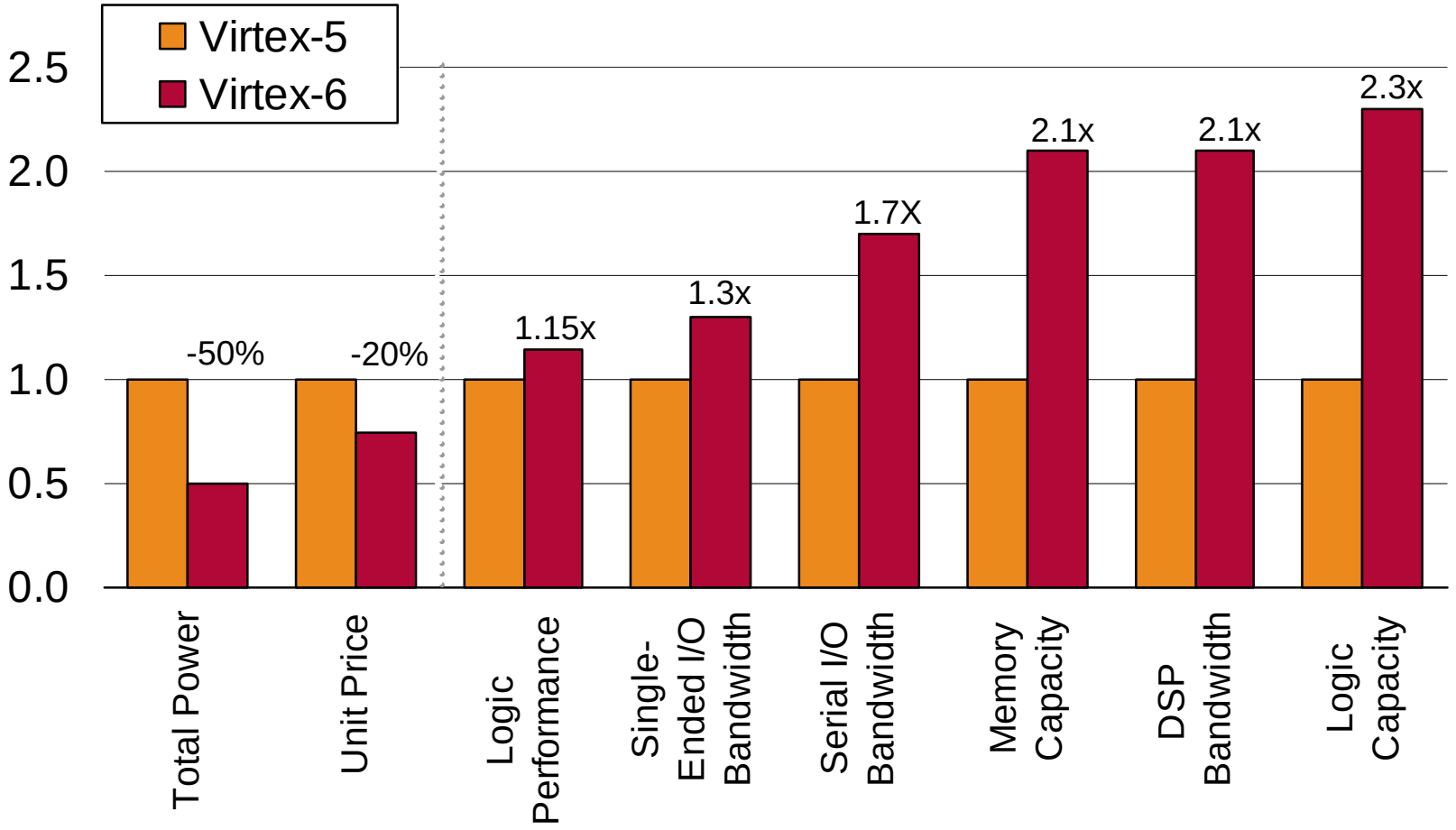
Virtex-6: Another Leap Forward



Half the power, 2x the Capability, Lower Cost

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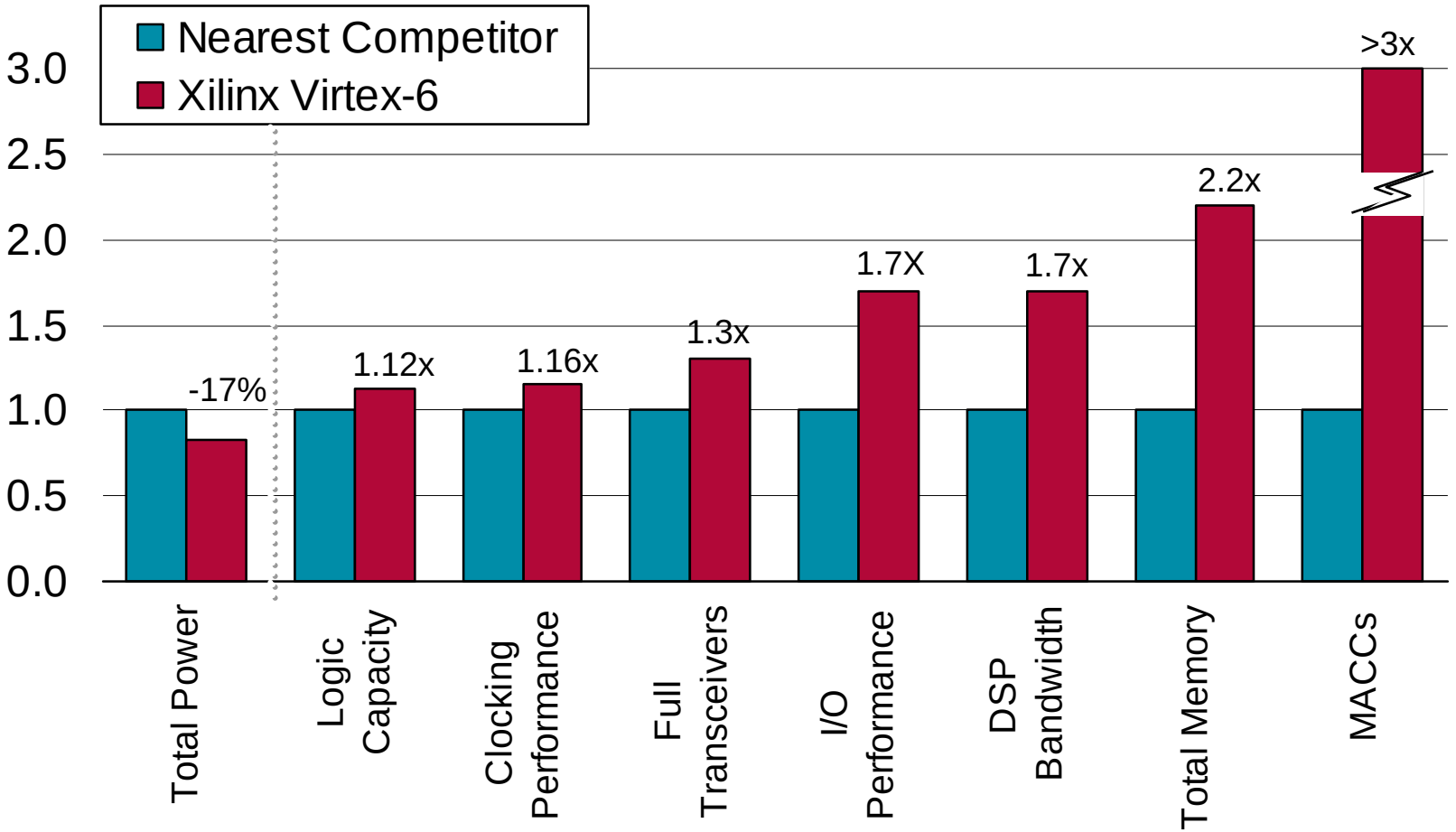
Virtex-6: Extends Leadership



Lower Power, Greater Capability

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Spartan-6 FPGAs Key Take Aways

- Lowest cost, low power FPGA
- 45nm, 9-layer metal process
- Two families, 11 devices
- Low cost, low power 3.2 Gbps serial connectivity
- 200+ early customer engagements
- Early access software support available today
- Shipping samples now, production Q4 CY09
- Rapid family deployment

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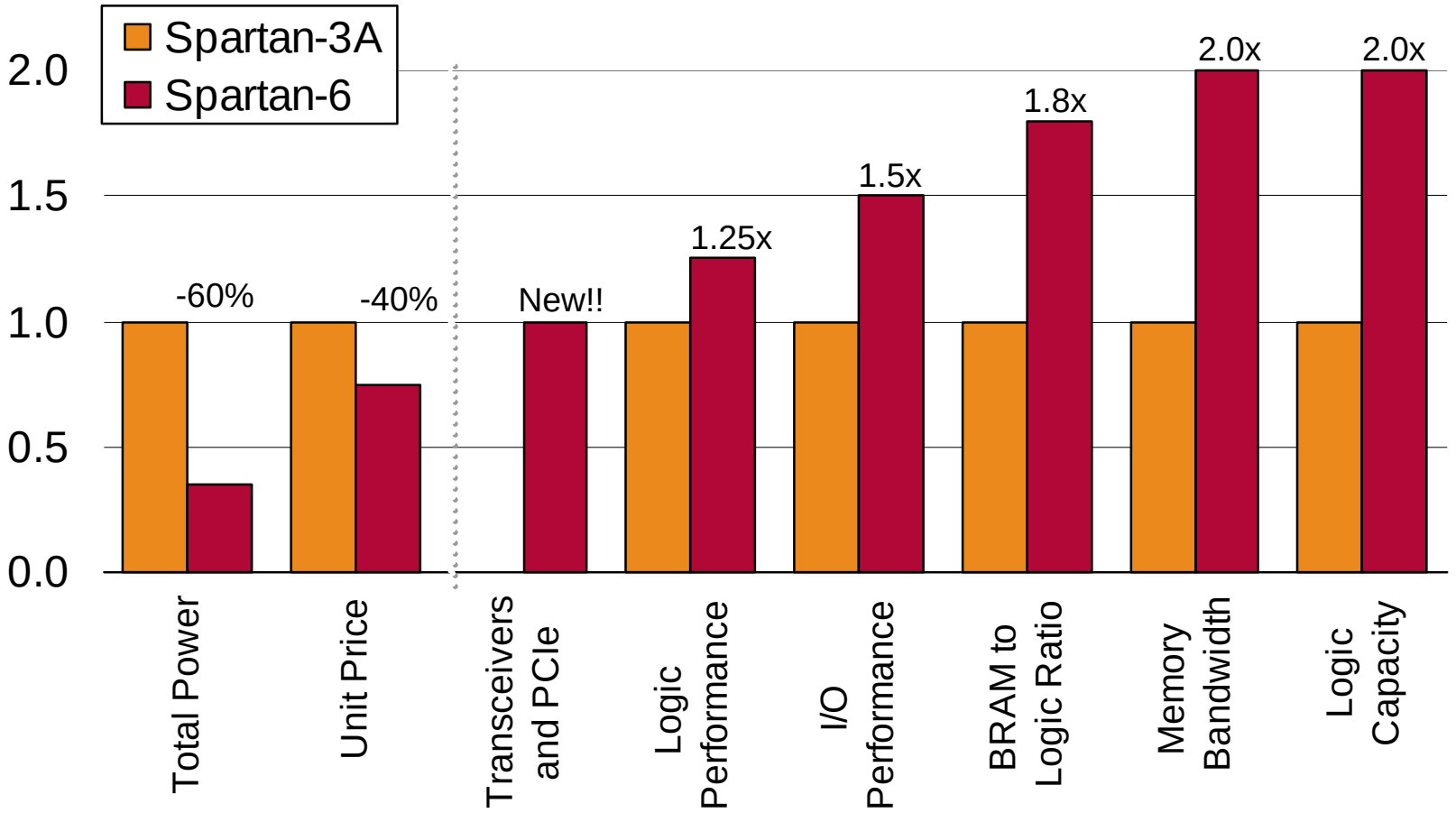
Spartan-6: A Huge Leap Forward



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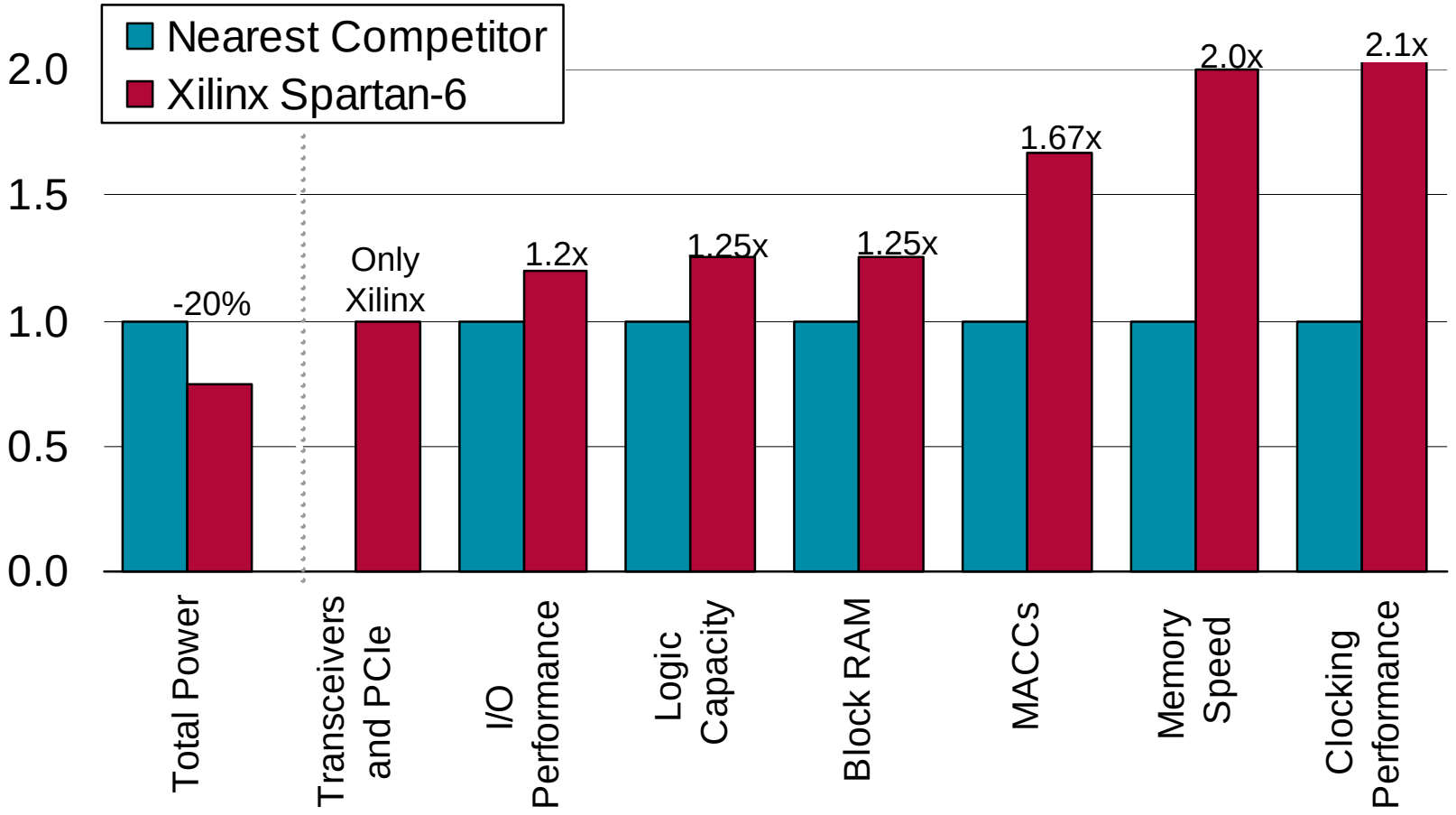
Spartan-6 FPGAs:
Reclaims High Volume Leadership



Lower Power, 2X the Capability, Lower Cost

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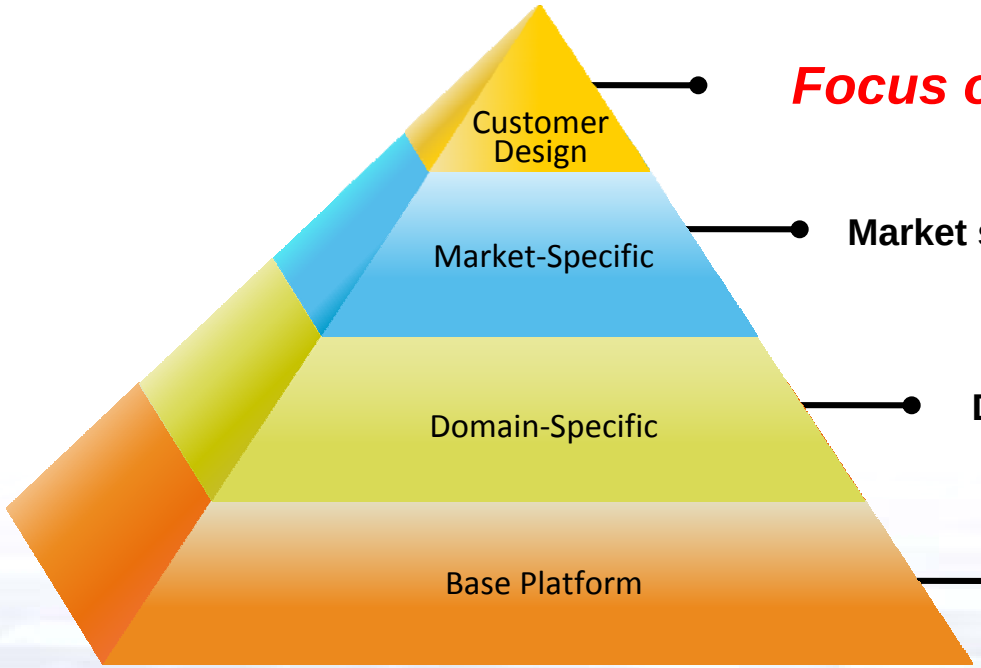

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Summary

Clear product leadership with next generation FPGA families

Targeted design platforms driving increased efficiencies for Xilinx and our customers

Virtex-6 and Spartan-6 FPGAs - the right products for the right time

Q&A