SUMMARY

xilinx

To our shareholders, customers, employees and partners

Xilinx delivered another record performance in fiscal 2001, which ended March 31, 2001. Total revenues increased 63 percent to $1.66 billion, outpacing all competitors and enabling us to capture three additional percentage points of share within the $4.1 billion Programmable Logic Device (PLD) industry, a fast-growing segment of the overall logic market. According to the market research firm Gartner Dataquest, Xilinx is now the world's fifth largest Application Specific Integrated Circuit (ASIC) supplier, up from seventh last year. Profitability measured by pro forma net income and revenue per employee also set company records in fiscal year 2001. On a pro forma basis, net income increased 51 percent to $382.9 million, while revenues per employee increased to $700,000, up from $600,000 at the end of last fiscal year.

A Message from the Chief Financial Officer

Xilinx has consistently innovated in the field of technology. We in investor relations also feel compelled to be innovative in the ways in which we communicate with each of you. During the past few years, the Internet has proven to be a very effective and low cost medium for us in providing meaningful information about Xilinx, so that you stay well informed.

As our shareholder base has continued to expand, the cost of printing a full-scale annual report for our now nearly 200,000 investors has become prohibitive. We hope you will all appreciate our move to this summary annual report, with an enclosed SEC Form 10-K. To continue to provide you with timely and concise information about our company, greater attention and effort is being placed on providing a more interactive and expansive online annual report that is easily printable. This approach helps us reduce costs. We would like your support in adopting this new way of receiving the annual report.

Sincerely,

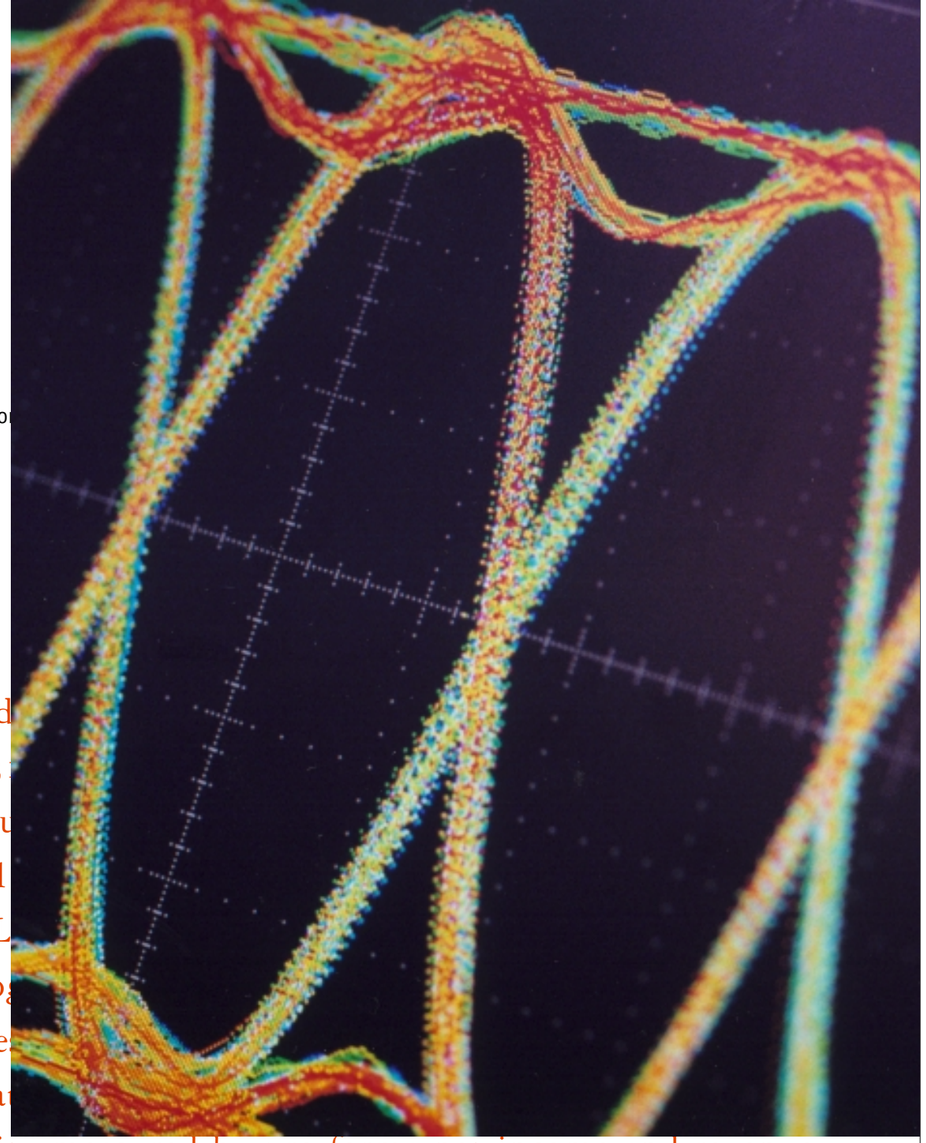
kris chellam
Senior Vice President, Finance and Chief Financial Officer

vere key beneficiaries of a strong
arkets, particularly communica-
mand for wireless communications
lendar year 2000, according to
hat of the overall semiconductor
of the overall logic industry, up
th expectations by our customers
unications carriers, significantly
signs of an inventory correction
weakened. By the March quarter,
MS) companies that manufacture
nately, this impacted the demand

r business structure allows us to
fabless company, we do not own
to leaders in this area, benefiting from their technical expertise while reducing the overhead costs associated with owning a fabrication plant. Additionally, we sell our products through distributors and sales representatives as opposed to employing a dedicated sales force. This means that a large portion of expenses associated with selling our products is variable since the sales representatives and distributors are paid only if they sell our products. This flexible business structure allows us to weather the inherent cyclicality of the PLD industry more profitably, while simultaneously allowing us to focus on our core competency – research and development.

Delivering Superior Solutions

Our focused research and development efforts continued to pay off in fiscal year 2001 as revenues from our flagship Virtex™ family of Field Programmable Gate Arrays (FPGAs) increased 320 percent from Fiscal 2000. The Virtex family now represents over 40 percent of total Xilinx revenues, up from 18 percent at the end of our previous fiscal year. During the March quarter, we announced our most important FPGA to date, the Virtex-II Platform



To our shareholders, custo

Xilinx delivered
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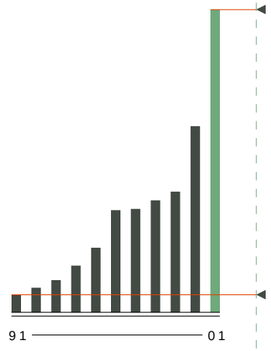
Net Revenues

$ Millions / FY 1991 – 2001



33%

Compound Annual Growth Rate

01	$1,659.4
00	1,021.0
99	662.0
98	613.6
97	568.1
96	560.8
95	355.1
94	256.4
93	178.0
92	135.8
91	97.6

During the last few years, the PLD industry and Xilinx were key beneficiaries of a strong global economy and unprecedented growth in our end markets, particularly communications. The build-out of the Internet infrastructure and the demand for wireless communications fueled PLD industry growth of nearly 60 percent in calendar year 2000, according to Gartner Dataquest. This growth rate is almost double that of the overall semiconductor industry. The PLD industry now represents 16 percent of the overall logic industry, up from 13 percent in calendar 1999. However, initial growth expectations by our customers slowed when their customers, particularly the telecommunications carriers, significantly reduced capital expenditures. Xilinx experienced the first signs of an inventory correction in the December quarter when orders from our customers weakened. By the March quarter, our customers and the Electronic Manufacturing Service (EMS) companies that manufacture their products, had accumulated excess inventories. Ultimately, this impacted the demand for Xilinx products, spurring a high rate of cancellations.

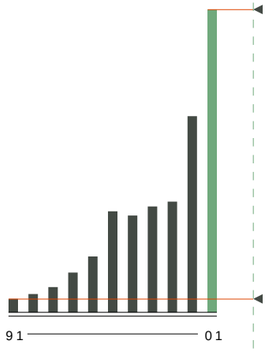
While the extent of this correction remains uncertain, our business structure allows us to retain profitability through the economic downturn. As a fabless company, we do not own or operate wafer fabrication facilities. Rather, we outsource to leaders in this area, benefiting from their technical expertise while reducing the overhead costs associated with owning a fabrication plant. Additionally, we sell our products through distributors and sales representatives as opposed to employing a dedicated sales force. This means that a large portion of expenses associated with selling our products is variable since the sales representatives and distributors are paid only if they sell our products. This flexible business structure allows us to weather the inherent cyclicality of the PLD industry more profitably, while simultaneously allowing us to focus on our core competency – research and development.

Delivering Superior Solutions

Our focused research and development efforts continued to pay off in fiscal year 2001 as revenues from our flagship Virtex™ family of Field Programmable Gate Arrays (FPGAs) increased 320 percent from Fiscal 2000. The Virtex family now represents over 40 percent of total Xilinx revenues, up from 18 percent at the end of our previous fiscal year. During the March quarter, we announced our most important FPGA to date, the Virtex-II Platform

Operating Income

$ Millions / FY 1991 – 2001



36%

Compound Annual Growth Rate

01	$497.1[a]
00	322.2
99	182.0
98	173.9
97	159.1
96	165.8
95	92.0
94	65.2
93	41.6
92	30.1
91	22.6

a ... Xilinx results are being reported on a pro forma basis which excludes acquisition related expenses and gains/losses on strategic investments.

FPGA. The Platform FPGA takes an evolutionary leap over existing FPGA technology by embedding intellectual property (IP) cores of silicon, or hard-IP, into the flexible fabric of our Virtex-II architecture. Virtex-II is our latest generation Virtex product, which we began shipping during the March quarter. By the end of calendar 2001, we expect to introduce Platform FPGAs with two types of embedded hard-IP: IBM's PowerPC processor and Conexant's high-speed transceiver technology.[1] The PowerPC processor is the most widely used processor in the networking, storage and telecommunications industries. These industries represent a substantial portion of total Xilinx sales. High-speed transceiver technology is critical for tomorrow's datapath-intensive applications, which require ultra-high performance as well as the ability to interface with a variety of emerging standards such as Infiniband, Fibre Channel and Gigabit Ethernet. Today, the processor and transceiver technologies exist in the form of discrete components in customer systems. By integrating these technologies into an FPGA, our customers will enhance their system performance, reduce power consumption and save valuable board space, resulting in what we believe to be the best possible solution at the lowest incremental cost.

We remain strongly committed to our software-based IP cores, which offer designers the ultimate flexibility. Currently, we offer customers over 200 cores for telecommunications, video and image processing, encryption and Digital Signal Processing (DSP), to name a few. In November, we unveiled the XtremeDSP initiative, demonstrating our commitment to providing high-performance DSP solutions. Xilinx FPGAs are uniquely suited to very high-speed DSP processing for use in applications such as cellular base stations, video streaming and High-Definition TV (HDTV), delivering speeds up to 70 times the performance of conventional DSP solutions. Software plays a critical role in PLD design and provides extremely high value to our customers. Recognizing its importance, Xilinx invests over 40 percent of research and development dollars in software design and employs 300 software engineers – more than all other pure-play PLD companies combined. Xilinx consistently makes software available before silicon, giving customers an important time-to-market advantage. Additionally, the speed of our software increases dramatically with each new release. As measured in runtime, Xilinx software is 60 times faster today than it was five years ago, substantially improving the overall productivity of our customers.

Product Highlights.

Alliance 3.1i software tools

In June 2000, Xilinx released its Alliance 3.1i software tools to further extend Xilinx's leadership in accelerating design completion, coupled with the highest clock frequencies available for FPGAs. This software also includes industry-leading features for multi-million gate designs, such as modular and incremental design.

XtremeDSP

In November 2000, Xilinx unveiled its XtremeDSP initiative, demonstrating Xilinx's commitment to providing high-performance DSP solutions. Xilinx FPGAs are uniquely suited to very high-speed DSP processing used in applications such as cellular base stations, video streaming and HDTV, delivering speeds of up to 70 times the performance of conventional DSP solutions.

Virtex series Platform FPGAs

In January 2001, Xilinx launched its next generation Virtex series Platform FPGAs. Based on the new Virtex-II architecture, this important evolutionary step allows the integration of both soft and hard intellectual property cores into an FPGA. The Virtex-II family members range in density from 40,000 up to 10 million system gates and are manufactured using 0.15-micron process technology. The first members of the Virtex-II family are currently shipping with the rest of the family expected to be available by the end of calendar 2001.

Home Networking

During Fiscal 2001, Xilinx spearheaded a Home Networking initiative aimed at educating FPGA and ASIC designers on evolving standards and technologies in the emerging home networking market. Xilinx Spartan FPGAs benefit greatly from the growth in the home networking space and are used increasingly in applications such as SOHO routers, video on demand and wireless LANs. In fiscal 2001, sales from Spartan family FPGAs increased nearly 160 percent compared to fiscal 2000.

According to Gartner Dataquest, the PLD segment of the overall logic industry grew from 13 percent in 1999 to 16 percent in 2000. Additionally, Xilinx gained three percentage points of share in the PLD industry and is now the world's fifth largest supplier of ASICs.

XILINX

Strategic Alliances.

IBM ..... Xilinx and IBM formed a powerful alliance that combines several key technologies such as PowerPC processors, FPGAs and next generation process technology to create industry-leading products and solutions. These products are expected to expand the available markets for both companies in the areas of communications, storage and consumer applications.

CONEXANT ..... Prior to the acquisition of RocketChips, Xilinx entered into a strategic relationship with Conexant to license industry-leading multi-gigabit serial technology. This technology will make it easier for designers to link together multiple high-speed chips or systems, thereby offering unprecedented integration and system performance.

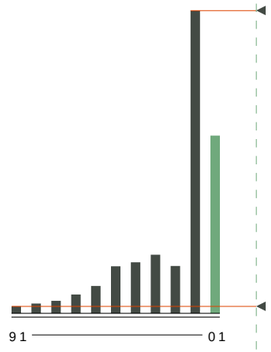
MATHWORKS ..... Xilinx and Mathworks formed an alliance to define and develop leadership software products and tools to help software designers more easily use FPGAs for high-performance DSP applications. The scope of the alliance includes joint development, marketing and sales.

WINDRIVER ..... Xilinx and WindRiver announced a multi-faceted alliance for developing upgradable embedded systems for smart, networked devices already deployed in the field. The agreement will enable developers to create hardware upgradable embedded systems. It is the first time that developers will have operating system-level tools to create remotely upgradable devices using PLDs.

3.

Net Income

$ Millions / FY 1991 – 2001



37%

Compound Annual Growth Rate

01	$382.9[a]
00	652.5[b]
99	102.6
98	126.6
97	110.4
96	101.5
95	59.3
94	41.3
93	27.2
92	21.3
91	15.9

a ... Xilinx results are being reported on a pro forma basis which excludes acquisition related expenses and gains/losses on strategic investments.

b ... includes a $398,089 net of tax gain from UMC/USIC merger.

Partnerships On All Fronts

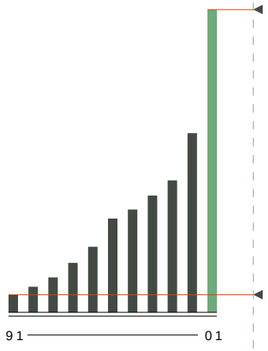
The pace of our innovation remains the fastest in the PLD industry. In addition to the skills and dedication of our own people, we accelerated our progress by building strategic partnerships with other technology leaders.

Our primary foundry partners are International Business Machines (IBM), United Microelectronics Company (UMC) and Seiko Epson. Our alliance with IBM allows us early access to the industry's most advanced technologies. Last year, Xilinx was first to market using IBM's copper-based technology, and this year, we plan to introduce the first FPGA embedding IBM's PowerPC processor.[1] At the same time, IBM benefits from our proprietary FPGA technology, enabling more rapid yield improvement on new technologies. The partnership with our foundry partner, UMC, has enabled Xilinx to be consistently first to market with advanced process technologies including 0.35-micron, 0.25-micron, 0.18-micron and 0.15-micron. Additionally, Xilinx recently became the first PLD company to manufacture chips on 300mm wafers. Mainstream wafer production today is on 200mm wafers. Moving to 300mm wafers significantly reduces production costs, enabling Xilinx to make even more aggressive inroads into the overall ASIC market.[2]

As customer systems become more sophisticated and time-to-market pressures more acute, software plays a pivotal role in the design process. Not only does Xilinx employ more software engineers than any other PLD company, but the breadth of our partnerships is unmatched in the PLD industry segment. Currently, we have a foundation of long-standing partnerships in place with nearly 200 companies in Electronic Data Automation (EDA), third-party IP and design software. This year we expanded these partnerships to include a collaboration with WindRiver, a leading provider of software and services for embedded systems applications. We expect this collaboration to yield a unified system software/hardware solution for the Platform FPGA. Additionally, Xilinx formed a partnership with The Mathworks, which gives nearly 500,000 DSP designers the ability to design FPGAs using existing DSP design methodologies. This is important, as it will expose a large number of DSP designers to FPGAs for the first time. In the areas of software, IP cores and services, our efforts are unsurpassed in the industry.

R + D Investments

$ Millions / FY 1991 – 2001



33%

Compound Annual Growth Rate

01	**$208.7**
00	123.6
99	90.9
98	80.5
97	71.1
96	64.6
95	45.3
94	34.3
93	24.3
92	17.7
91	12.4

New Market Opportunities

The year 2000 was an active year for acquisitions. Our acquisition philosophy is focused on acquiring new technology or leading expertise that is critical to our growth. One of the best examples of this is our acquisition of RocketChips, Inc., a leading developer of ultra-high-speed transceivers serving the networking, enterprise storage and wireless and wired telecommunications markets. This technology will address critical needs of these markets' next-generation applications that are estimated to exceed $6 billion. The combination of this high-speed transceiver technology and our market-leading FPGA solutions promises to provide dramatic system-level benefits, while expanding our presence in our customers' systems.[3] Moreover, we are excited by the addition of RocketChips' specialized technical expertise to our world-class research and development team.

Home networking and digital consumer electronics also represent exciting new market opportunities for Xilinx chips. It is clear that the home is the next market in which networking technologies will be broadly deployed. In March 2001, Xilinx launched a home networking initiative aimed at educating FPGA designers about evolving technologies. As part of this initiative, Xilinx is hosting global educational seminars for engineers, providing a technical overview of current state-of-the-art home networking technologies as well as insights into future product and technology directions. Additionally, Xilinx has developed the industry's first web portal dedicated exclusively to the home networking market (www.xilinx.com/esp). Xilinx Spartan™ FPGAs are strong beneficiaries of the growth in this space and are used increasingly in applications such as video on demand, Small Office Home Office (SOHO) routers and wireless Local Area Networks (LANs). In Fiscal 2001, sales from Spartan family FPGAs increased nearly 160 percent compared to fiscal 2000. In the realm of digital consumer electronics, the low-power CoolRunner™ family of Complex Programmable Logic Devices (CPLDs) continues to gain ground with design wins in applications such as Wireless LAN cards, high-end cell phones and Personal Digital Assistant (PDA) add-in cards. Sales from this CPLD family more than doubled in fiscal year 2001.

Acquisitions.

ROCKETCHIPS ..... Xilinx acquired RocketChips for its ultra-high-speed gigabit transceiver technology. This technology enables very high-bandwidth data rates required for next generation networking, telecommunications and enterprise storage solutions. These markets collectively represent an incremental market opportunity of over $6 billion.

DYNACHIP ..... The acquisition of Dynachip's technical talent and intellectual property (IP) helped Xilinx create leading edge I/O technology for our latest Virtex-II devices and beyond.

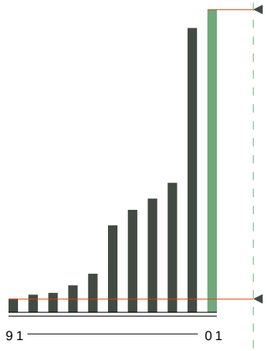
COOLRUNNER ..... The acquisition of Philips' CoolRunner CPLD family opened up a new and fast growing market for Xilinx. This family of low power products is ideal for battery-operated mobile computing devices and Internet appliances. There is no low power rival to the Xilinx CoolRunner family.

INTEGRAL DESIGN ..... We acquired Integral Design, a design service company in Dublin, Ireland for their expertise in the areas of System-on-a-Chip and embedded software. This expertise, combined with Xilinx technology, will help Xilinx customers get their complex designs to market faster.

LAVA LOGIC ..... We acquired Lava Logic to accelerate the development of tools that will eventually allow software engineers to design FPGA hardware without needing to learn about hardware technology. Software engineers will be able to write in their familiar "C code" language and then compile their designs efficiently into a Xilinx FPGA.

Total Assets

$ Millions / FY 1991 – 2001



01	**$2.502.2**
00	2.348.6
99	1.070.2
98	941.2
97	847.7
96	720.9
95	320.9
94	226.2
93	162.9
92	146.6
91	111.6

36%

Compound Annual Growth Rate

Net Result

The initiatives we have put in place, combined with our strategic partnerships and acquisitions have a single focus – to continue extending our leadership in all facets of the PLD and ASIC industries. Xilinx technology will continue to provide greater flexibility, faster time to market and superior overall solutions for our customers. Ultimately, we believe that Xilinx can become the solution of choice for most electronic equipment suppliers.

Over the past few years, we have cemented our market leadership in the PLD industry with a strong product portfolio. Historically, companies with the strongest product cycles are best able to improve their competitive position when emerging from cyclical downturns. In fiscal year 2002, we plan to continue leveraging our fabless business structure, while focusing on operational efficiency. This summary annual report, for example, is a much more cost-efficient way to communicate with our investors when compared with a traditional annual report. For a more comprehensive update on Xilinx, our performance, our products and our markets, I encourage you to explore our online annual report by visiting the investor relations website at http://www.investor.xilinx.com.

I will close by thanking our shareholders, customers, employees and partners. My belief in Xilinx, our technology, our people and our growing opportunities has never been stronger.

willem p. roelandts
President and Chief Executive Officer

1 This forward-looking statement is subject to risks and uncertainties including the timely introduction of the Platform FPGA into the marketplace.

2 This forward-looking statement is subject to risks and uncertainties including the timely migration to 300mm wafers and the continued customer acceptance of our products.

3 This forward-looking statement is subject to risks and uncertainties including the timely introduction of our products into the marketplace as well as customer acceptance of our new products.

Corporate Information.

Board of Directors

Bernard V. Vonderschmitt
Chairman of the Board
Xilinx, Inc.

Willem P. Roelandts
President and
Chief Executive Officer
Xilinx, Inc.

John L. Doyle
Consultant

Jerald G. Fishman
President and
Chief Executive Officer
Analog Devices, Inc.

Philip T. Gianos
General Partner
InterWest Partners

William G. Howard, Jr.
Consultant

Frank Seiji Sanda
Chairman, President and
Chief Executive Officer
Japan Communications, Inc.

Dennis L. Segers
Senior Vice President
and General Manager
Xilinx, Inc.

Richard W. Sevcik
Senior Vice President
Xilinx, Inc.

Elizabeth Vanderslice
Vice President and
General Manager
Terra Lycos, Inc.

Corporate Officers

Willem P. Roelandts
President and
Chief Executive Officer

William S. Carter
Vice President and
Chief Technical Officer

Kris Chellam
Senior Vice President,
Finance and
Chief Financial Officer

Alexander Glass
Sector Vice President
Europe, Middle East
and Africa

Steven D. Haynes
Vice President
Worldwide Sales

Makoto Kawakami
President
Xilinx, K.K.

Motohiro Kitajima
Chairman
Xilinx, K.K.

Thomas Lavelle
Vice President
General Counsel
and Secretary

Paul McCambridge
Vice President and
Managing Director
Xilinx, Ireland

Randy Ong
Vice President
Worldwide Operations

Dennis L. Segers
Senior Vice President
and General Manager
Advanced Products Group

Richard W. Sevcik
Senior Vice President
IP, Software and
Services Group

Sandra L. Sully
Vice President and
Chief Information Officer

Sandeep S. Vij
Vice President, Marketing
and General Manager
General Products Division

Evert A. Wolsheimer
Vice President and
General Manager
CPLD Division

Margaret B. Wynn
Vice President
Worldwide Human
Resources

Worldwide Corporate Offices

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Kowloon
Hong Kong
tel: 852-2424-5200

Corporate Information

Independent Auditors
Ernst & Young LLP
San Jose, CA

Common Stock
Xilinx's Common Stock is listed on the NASDAQ National Market System under the symbol XLNX. As of March 31, 2001, there were approximately 1,515 shareholders of record. Since many holders' shares are listed under their brokerage firms' names, the actual number of shareholders is estimated by the Company to be over 195,000.

Inquiries Concerning the Company
If you have questions regarding Xilinx's operations, recent results or historical performance, or if you wish to receive an investor package, please contact:

Investor Relations
www.investor.xilinx.com
Email: ir@xilinx.com
Phone: 800-836-4002

The toll-free shareholder service number listed above allows shareholders to obtain quarterly and annual financial reports in addition to the Company's latest new releases by voice recording, fax or mail. Copies of the Xilinx Annual Report including the Report on Form 10-K are available to all shareholders without charge.

Transfer Agent and Registrar
Please send change of address and other correspondence to:
Equiserve L.P.
Shareholder Services
P.O. Box 8040
Boston, MA 02266-8040
Phone: (781) 575-3120

Annual Meeting
The Xilinx annual meeting of stockholders will be held at 11:00 am on August 9, 2001 at Xilinx, Inc., 2100 Logic Drive, San Jose, CA.

Dividend Information
Xilinx has never paid a cash dividend on its Common Stock and intends to continue this policy for the foreseeable future.

Twelve month closing stock price range:

April 2000 to March 2001:
$35.13 – $97.94

Shares Outstanding at Fiscal year end:
332.6M shares

Average Daily Trading Volume Fiscal 2001:
8.3M shares

XILINX®

see the expanded annual report online at
www.investor.xilinx.com

Item 1. Business

Items 1 and 3 of this 10-K contain forward-looking statements concerning our development efforts, strategy, new product introductions, backlog and litigation. These statements involve numerous risks and uncertainties including those discussed throughout this document as well as under "Factors Affecting Future Operating Results" in Item 7. Forward looking statements can often be identified by the use of forward looking words, such as "may," "will," "could," "should," "expect," "believe," "anticipate," "estimate," "continue," "plan," "intend," "project," or other similar words.

General

Xilinx, Inc. (Xilinx or the Company) designs, develops and markets complete programmable logic solutions, including advanced integrated circuits (ICs), software design tools, predefined system functions delivered as cores of logic design services and field engineering support. Our programmable logic devices (PLDs) include field programmable gate arrays (FPGAs) and complex programmable logic devices (CPLDs). These devices are standard products that our customers program to perform desired logic functions. Our products are designed to provide high integration and quick time-to-market for electronic equipment manufacturers primarily in the telecommunications, networking, computing, industrial, and consumer markets. Our products are sold globally through a network of independent sales representatives, distributors, and to original equipment manufacturers ("OEMs").

Competitive pressures compel manufacturers of electronic systems to accelerate their products' introduction to market. Customer requirements for improved functionality, performance, reliability and lower cost are addressed through the use of components that integrate ever larger numbers of logic gates onto a single integrated circuit. Such integration often results in greater speed, smaller die size, lower power consumption and reduced costs. The rapid proliferation of the Internet and wireless communications continues to fuel the demand for faster integrated circuits. At the same time, tremendous pressure is placed on electronic equipment manufacturers' product life cycles. Due to their functionality and reprogrammability, our PLDs enable electronic equipment manufacturers to effectively respond to these evolving market trends.

We were organized in California in February 1984 and in November 1985 were reorganized to incorporate our research and development limited partnership. In April 1990, we reincorporated in Delaware. Our corporate facilities and executive offices are located at 2100 Logic Drive, San Jose, California 95124 and our website is www.xilinx.com.

Our fiscal year ends on the Saturday nearest March 31. For ease of presentation, March 31 has been utilized as the fiscal year-end for all financial statement captions. Fiscal 2001 ended on March 31, 2001 while fiscal 2000 and 1999 ended on April 1, 2000 and April 3, 1999, respectively.

Products

Integral to the future success of our business is the timely introduction of new products which address customer requirements and compete effectively on the basis of price, functionality, and performance. Xilinx programmable logic solutions help minimize risks for manufacturers of electronic equipment by shortening the time required to develop products and introduce them to market. Customers can design and verify their unique circuits in Xilinx programmable devices much faster than they could by choosing traditional methods such as mask-programmed, fixed logic gate arrays. Moreover, because Xilinx devices are standard parts that need only to be programmed, customers are not required to wait for prototypes or pay large non-recurring engineering costs. Xilinx silicon products, software solutions, and technical support make up the total solution delivered by Xilinx. The software component of this solution is critical to the success of every design project. Our Software Solutions provide powerful tools which make designing with programmable logic easy. Push button design flows, integrated on-line help, multimedia tutorials, plus high performance automatic and auto-interactive tools, help designers achieve optimum results. We offer the industry's broadest array of programmable logic technology and EDA integration options allowing us to deliver unparalleled design flexibility. Xilinx has also developed a technology that enables the hardware in Xilinx-based systems to be upgraded remotely over any kind of network including the Internet even after the equipment has been shipped to a customer. Such Xilinx Online Upgradable Systems allow equipment manufacturers to remotely add new features and capabilities to installed systems or repair problems without having to physically exchange hardware.

Programmable Logic Devices

We currently classify our product offerings into four categories by manufacturing process technology. Base products consist of our mature product families that are currently manufactured on technologies of 0.6-micron and greater; this includes the XC3000, XC3100, and XC4000 families. Mainstream products are currently manufactured on 0.35 and 0.5-micron technologies and include the XC4000E, XC4000EX, XC4000XL, XC5200, XC9500, XC9500XL, Spartan™ and CoolRunner™ product lines. Advanced products include our newest technologies manufactured on 0.25-micron and smaller, which include the XC4000XV, XC4000XLA, XC9500XV, SpartanXL™, Spartan-II™, Virtex™, Virtex-E™, and Virtex-II™ product lines. Support products make up the remainder of our product offerings and include configuration solutions, software, design services, and support.

Virtex-II™ Platform FPGAs:

The Virtex-II Platform FPGA family, introduced in January 2001, is a complete programmable solution that allows digital system designers to rapidly implement a single-chip solution with densities from 40,000 up to 10 million system gates. The Virtex-II family is the first Platform FPGA to incorporate the IP-Immersion™ fabric that not only provide the ability to integrate a variety of soft intellectual property (IP), but also has the capability of embedding hard IP cores such as processors and Gigabit serial I/Os in future Virtex-II families schedule for late 2001. The Virtex-II solution was developed to enable rapid development of data communications and digital signal processing (DSP) systems. The unique features of the revolutionary Virtex-II architecture make it ideal for optical networking products, storage area networks (SANs), voice-over-Internet-protocol (VoIP), video broadcasting, medical imaging, cellular

base-stations, and Internet infrastructure products. The Virtex-II devices will be delivered on 0.15-micron process technology.

Virtex™ FPGAs:

The Virtex-EM Extended Memory (Virtex-EM) FPGA, introduced in March 2000, extends the Virtex-E architecture. The Virtex-EM FPGA family consists of two devices that have a high RAM-to-logic gate ratio, over 1 million bits of block RAM, that is targeted for specific applications such as gigabit-per-second network switches and high definition graphics. The Virtex-EM devices are the first FPGAs to be manufactured using an advanced copper process.

The Virtex-E™ FPGA family, introduced in September 1999, includes a two million system gate device and supports twice the system-gate density and has a 50 percent higher I/O performance than the original Virtex™ FPGAs. The Virtex-E™ family consists of 11 members, from 50,000 system gates to 3.2 million system gates. The Virtex-E™ FPGAs, delivering new performance and density attributes that were only previously addressed by ASIC solutions, are targeted for next generation networking and telecommunication applications. Virtex-E™ FPGAs with 1.8-volt operation are the first programmable logic devices delivered on 0.18-micron process technology, which was jointly developed by Taiwan's United Microelectronics Corporation (UMC) and Xilinx. The improved process directly contributes to a substantial performance gain. The Virtex-E™ family also represents the industry's first programmable logic architecture with 210 million transistors on a single device.

The Virtex™ FPGA series, announced in October 1998, includes the industry's first million-gate FPGA. Nine Virtex™ devices are currently in production. The Virtex™ devices with 2.5-volt operation are found in traditional programmable logic applications such as networking or telecommunications, and in applications like storage area networks, routers, high end servers, switching equipment, cellular base stations, and High Definition Television (HDTV) infrastructure. The Virtex™ devices range from 50,000 to 1,000,000 system gate densities with 200 MHz chip-to-chip performance and offer system-level integration capabilities. The Virtex™ family delivers the first fully programmable alternative to high density system-level Application Specific Integrated Circuits (ASIC) design.

XC4000 FPGAs:

The XC4000 family, introduced in 1990, was the first FPGA offering on-board distributed RAM. The XC4000 became the industry standard and was the fastest growing programmable logic family in history until the Virtex family was introduced in October 1998.

The XC4000XL family has 11 members shipping in volume ranging in density from 2,000 to 180,000 system gates. The XC4000XLA family expands on the XC4000XL architecture with reduced power consumption and improved performance. The XC4000XLA family has eight members shipping in volume and ranges in density from 30,000 to 180,000 system gates. The XC4000XV is a 2.5-volt FPGA family that utilizes 0.25-micron technology. The family has four members with up to 500,000 system gates. The XC4000XV features system performance of over 100 MHz while minimizing power consumption. The 2.5-volt XC4000XV family extends and builds on the successes of the 5-volt XC4000 and the 3-volt XC4000XL series.

Spartan™ FPGAs:

The Xilinx Spartan™ and SpartanXL™ FPGA families are derived from the XC4000 architecture. These families feature low-cost ASIC replacement with densities ranging from 5,000 to 40,000 system gates. In January 2000, we announced the Spartan-II™ family, our newest generation of high-volume FPGAs, which is based on the Virtex architecture. Spartan-II™ devices are designed to be low cost programmable replacements for ASICs and application specific standard products (ASSPs). New features in the Spartan-II™ family address a larger range of cost-sensitive high-volume applications and open up new consumer market opportunities for programmable logic.

CPLDs:

The XC9500 and XC9500XL families offer in-system programmability for 5.0-volt and 3.3-volt systems, respectively. The XC9500XV is a 2.5-volt in-system programmable CPLD family with significantly reduced power consumption.

In August 1999 we acquired Philips Semiconductors' line of low power complex programmable logic devices (CPLDs) called the CoolRunner® family of devices. The CoolRunner line is the first family of CPLD products to combine very low power with high speed, high density, and high I/O counts in a single device. CoolRunner® CPLDs also use far less dynamic power during actual operation compared to conventional CPLDs, an important feature for today's mobile computing applications.

Software, Cores & Support

We offer complete software design tool solutions which enable customers to implement their design specifications into our PLDs. These software design tools combine a powerful technology with a flexible, easy to use graphical interface to help achieve the best possible designs within each customer's project schedule, regardless of the designer's experience level.

We offer three complementary software design tool solutions. Xilinx Foundation Series software provides designers with a complete, ready-to-use design solution based on industry-standard hardware description languages (HDLs). We offer this fully integrated software solution for those customers new to designing with PLDs or desiring a low cost approach. The Foundation ISE™ (Integrated Synthesis Environment) software, introduced in the fourth quarter of fiscal year 2001, is Xilinx's next generation design environment. Foundation ISE software provides a design environment which integrates the HDL design flow, synthesis, and optimization to ensure a comprehensive integrated design flow for designers to increase productivity. The Alliance Series is tailored for designers who want maximum flexibility to integrate their programmable logic design into their existing EDA environment and methodology. With interfaces to over fifty EDA vendors, the Alliance Series Software allows users to select tools with which they are most familiar, thereby increasing their productivity and shortening their products design cycles.

Xilinx offers two Web-based Design solutions giving designers the ability to engage in digital design activities on-line using either our application servers or download design and implementation software modules for use in their own design environment. The WebFITTER is a free Web-Based design tool that allows system designers to evaluate their designs using our XC9500/XL/XV and CoolRunner Series CPLDs. WebPACK™ solutions are a collection of free downloadable software modules. Customers can register and download any of the WebPACK™ modules to complete designs using the Xilinx XC9500/XL/XV, CoolRunner Series CPLD, the entire Spartan-II FPGA family designs and the 300,000 system gate Virtex XCV300E FPGA.

We also offer intellectual property, cores of logic, for commonly used complex functions such as digital signal processing (DSP), bus interfaces, processors, and peripheral interfaces. Using logic cores, available from Xilinx and third party AllianceCORE partners, customers can shorten development time, reduce design risk and obtain superior performance for their designs. Additionally, our CORE Generator system allows customers to implement intellectual property cores into our PLDs. It offers a simple user interface, complete cataloging of available cores, easy selection of parameter-based cores optimized for our FPGAs, and features an interface to third-party system level DSP design tools. Further, Xilinx's IP Center Internet portal offers customers the ability to purchase on line

the latest intellectual property cores and reference design via Smart Search for faster access.

To extend our customers' technical capabilities and accelerate our customers' design time in the race to market, we offer Xilinx Global Services which consists of education, product, and design services along with the support.xilinx.com online. At Support.xilinx.com, customers can find training courses, discussion forums access to an experienced Xilinx team for assistance in troubleshooting and design issues. To grow the emerging home networking market, we also introduced the Xilinx eSP website in the fourth quarter of fiscal 2001. This web portal is a comprehensive resource offering designers information such as reference designs and intellectual property. It is the industry's first web portal dedicated to accelerating the design and development of consumer products based upon emerging standards and protocols.

Our software design tools operate on desktop computer platforms, including personal computers with Microsoft Windows '95, '98, 2000, and NT operating systems, and on workstations from IBM, HP and Sun Microsystems.

The net revenues from Software, Cores & Support were $21.2 million, $15.3 million, and $13.0 million in fiscal 2001, 2000, and 1999, respectively.

Research and Development

Our research and development activities are primarily directed towards the design of new integrated circuits, the development of new software design tools and cores of logic, the development of advanced semiconductor manufacturing processes, and ongoing cost reductions and performance improvements in existing products. Our primary areas of focus have been: to introduce the industry's first 10 million system gate programmable system solution (Virtex-II Platform FPGA devices), a low-cost ASIC replacement FPGA solution (Spartan-II devices), development of CPLD products (XC9500/XL/XV & CoolRunner families), and releasing new versions of software design tools (Foundation Series ISE software) and cores of logic.

Our research and development challenge is to continue to develop new products that create cost-effective solutions for customers. In fiscal 2001, 2000, and 1999, our research and development expenses were $213.2 million, $123.6 million, and $90.9 million, respectively. Excluding a $4.5 million amortization expense of deferred stock compensation for acquiring RocketChips in fiscal 2001, the research and development expenditures were $208.7 million in fiscal 2001. We expect we will continue to make substantial investments in research and development. We believe technical leadership is essential to our future success and we are committed to continuing a significant level of research and development effort. However, there can be no assurance that any of our research and development efforts will be successful, timely or cost-effective.

Marketing and Sales

We sell our products through several industrial distributors, direct sales to manufacturers by independent sales representative firms, sales through franchised domestic distributors, and sales through foreign distributors. In order to provide service to existing customers and reach potential customers, we also utilize a direct sales management organization and field applications engineers (FAEs). Our independent representatives generally address larger OEM customers and act as a direct sales force, while distributors serve the balance of our customer base. Our sales and customer support personnel support all channels and consult with customers about their plans, ensuring that the right software and devices are selected at the beginning of a customer's project.

Avnet, Inc. and the Memec Group distribute our products worldwide and Nu Horizons Electronics provides additional regional sales coverage. From time to time, we may add or terminate distributors from our selling organization as we deem appropriate given the level of business. We believe distributors provide a cost-effective means of reaching a broad range of customers. Since our PLDs are standard products, they do not present many of the inventory risks to distributors as compared to custom gate arrays, and they simplify the requirements for distributor technical support.

We changed our accounting method during fiscal 1999 for recognizing revenue on all shipments to international distributors. While we previously deferred revenue on shipments to domestic distributors until the product was sold to the end user, we recognized revenue upon shipment to international distributors, net of estimated reserves for returns and allowances. Following the accounting change, revenue recognition on shipments to distributors worldwide is deferred until the products are sold to the end customer. Distributors have certain rights of return and price protection privileges on unsold product until the product is sold to the end customers.

Backlog and Customers

As of March 31, 2001, our backlog of purchase orders scheduled for delivery within the next three months was $126 million, after adjustments for estimated discounts. Backlog as of March 31, 2000 was $174.3 million, after adjustments for estimated discounts. Backlog amounts for both years include orders to distributors, which may receive price adjustments upon sale to end customers. Also, orders constituting our current backlog are subject to changes in delivery schedule or to cancellation at the option of the purchaser without significant penalty. Accordingly, although useful for scheduling production, backlog as of any particular date may not be a reliable measure of revenues for any future period.

No end customer accounted for more than 10% of revenues in fiscal years 2001, 2000, or 1999. Approximately 27%, 27%, and 20% of net revenues were recognized through our largest domestic distributor in 2001, 2000, and 1999, respectively. A second domestic distributor accounted for approximately 24%, 24%, and 17% of net revenues in fiscal 2001, 2000, and 1999, respectively. On a consolidated basis, at March 31, 2001, two distributors accounted for 44.1% and 28.6% of worldwide net revenues in fiscal 2001. (See Note 2 of Notes to Consolidated Financial Statements in Item 8 for Concentration of Credit Risk; see also Note 11 of Notes to Consolidated Financial Statements in Item 8 for geographic sales information.)

Wafer Fabrication

We do not directly manufacture processed wafers used for our products. Over the last several years, the majority of our wafer purchases have been manufactured by United Microelectronics Corporation, (UMC), UMC affiliated companies including our former joint venture, USIC, Seiko Epson Corporation (Seiko), and Taiwan Semiconductor Manufacturing Company (TSMC). Precise terms with respect to the volume and timing of wafer production and the pricing of wafers produced by the semiconductor foundries are determined by periodic negotiations between Xilinx and these wafer foundry partners.

Our strategy is to focus our resources on creating new integrated circuits and software design tools and on market development rather than on wafer fabrication. We continuously evaluate opportunities to enhance foundry relationships and/or obtain additional capacity from both our main suppliers as well as other suppliers of leading-edge process technologies. As a result, we have entered into agreements with UMC and Seiko as discussed below.

Xilinx, United Microelectronics Corporation (UMC) and other parties entered into a joint venture to construct a wafer fabrication facility in Taiwan, known as United Silicon Inc. (USIC). (See Note 4 of Notes to Consolidated Financial Statements in Item 8.) We made a

total cumulative investment of $107.1 million in USIC. In January 2000, as a result of the merger of USIC into UMC, our equity position in USIC was converted into shares of UMC which are publicly traded on the Taiwan Stock Exchange. We retain monthly guaranteed wafer capacity rights in UMC as long as we retain a percentage of our UMC shares. (See Note 4 of Notes to Consolidated Financial Statements in Item 8.)

In fiscal 1997, we signed a wafer purchasing agreement with Seiko Epson. (See Note 2 of Notes to Consolidated Financial Statements in Item 8.) This agreement was amended in fiscal 1998 and provided for an advance to Seiko Epson for $150.0 million. In conjunction with the agreement, $60.0 million was paid in fiscal 1997 and an additional $90.0 million was paid in fiscal 1998. Repayment of this advance is made in the form of wafer deliveries, which began during the fourth quarter of fiscal 1998 and ended during the second quarter of fiscal 2001. Specific wafer pricing was in U.S. dollars and was based upon the prices of similar wafers manufactured by other, specifically identified, leading-edge foundry suppliers.

In fiscal 2001, we signed a Licensing and Marketing Agreement (LMA) with International Business Machines Corporation (IBM), giving us the right to purchase certain specified amounts of wafers from IBM on a monthly basis. Presently, we are not purchasing a material number of wafers from IBM.

Sort, Assembly and Test

Wafers purchased by us are sorted by the wafer foundry, independent sort subcontractors or by us. Sorted wafers are assembled by subcontractors in facilities in South East Asian countries. During the assembly process, the wafers are separated into individual die, which are then assembled into various package types. Following assembly, the packaged units are tested by independent test subcontractors or by Xilinx personnel at our San Jose or Dublin, Ireland facilities.

Patents and Licenses

Through March 31, 2001, we held over 545 issued United States patents and we maintain an active program of filing for additional patents in the areas of software, IC architecture and design. We intend to vigorously protect our intellectual property. We believe that failure to enforce our patents or to effectively protect our trade secrets could have an adverse effect on our financial condition and results of operations. In the future, we may incur litigation expenses to enforce our intellectual property rights against third parties. There is no assurance that any such litigation would be successful. (See Legal Proceedings in Item 3 and Note 12 of Notes to Consolidated Financial Statements in Item 8.)

We have acquired various software licenses that permit us to grant object code sublicenses to our customers for certain third party software programs licensed with our software design tools. In addition, we have licensed certain software for internal use in product design.

Employees

Xilinx's employee population grew 38% during the past year. As of March 31, 2001, Xilinx had 2,678 employees compared to 1,939 at the end of the prior year. None of our employees are represented by a labor union. We have not experienced any work stoppages and believe we maintain good employee relations.

Competition

Our PLDs compete in the logic industry. The industries in which we compete are intensely competitive and are characterized by rapid technological change, product obsolescence, and continuous price erosion. We expect increased competition, both from our primary competitors, Altera Corporation and Lattice Semiconductor Corporation and from a number of new companies that may enter our market. We believe that important competitive factors in the programmable logic industry include:

- product pricing;
- product performance, reliability, power consumption, and density;
- the adaptability of products to specific applications;
- ease of use and functionality of software design tools;
- functionality of predefined cores of logic; and
- the ability to provide timely customer service and support.

Our strategy for expansion in the logic market includes continued introduction of new product architectures which address high volume, low cost applications as well as high performance, leading-edge density applications. In addition, we anticipate continued price reductions proportionate with our ability to lower the manufacturing cost for established products. However, we cannot assure that we will be successful in achieving these strategies.

Our major sources of competition are comprised of several elements:

- providers of high density programmable logic products characterized by FPGA-type architectures;
- providers of high volume and low cost FPGAs as programmable replacement for ASICs and application specific standard products (ASSPs).;
- providers of high speed, low density CPLD devices;
- the manufacturers of custom gate arrays;
- providers of competitive software development tools; and
- other providers of new or emerging programmable logic products.

We compete with high density programmable logic suppliers on the basis of device performance, the ability to deliver complete solutions to customers, device power consumption, and customer support by taking advantage of the primary characteristics of our PLD product offerings which include: flexibility, high speed implementation, quick time-to-market, and system level capabilities. We compete with ASIC manufacturers on the basis of lower design costs, shorter development schedules, and reduced inventory risk and field upgradability. The primary attributes of ASICs are high density, high speed, and low production costs in high volumes. We continue to develop lower cost architectures intended to narrow the gap between current ASIC production costs (in high volumes) and PLD production costs. As PLDs have increased in density and performance and decreased in cost due to the advanced manufacturing processes, they have become more directly competitive with ASICs. With the introduction of our Spartan family, which is Xilinx’s low cost programmable replacement for ASICs, we seek to grow by directly competing with other companies in the ASIC segment. Many of the companies in the ASIC segment have substantially greater financial, technical, and marketing resources than Xilinx. Consequently, there can be no assurance that we will be successful in competing in the ASIC segment. Competition among PLD suppliers and manufacturers of new or emerging programmable logic products is based primarily on price, performance, design, customer support, software utility, and the ability to deliver complete solutions to customers. Some of our current or potential competitors have substantially greater financial, manufacturing, marketing, distribution, and technical resources than we do. To the

extent that our efforts to compete are not successful, our financial condition and results of operations could be materially adversely affected.

The benefits of programmable logic have attracted a number of companies to this market. We recognize that different applications require different programmable technologies, and we are developing architectures, processes, and products to meet these varying customer needs. Recognizing the increasing importance of standard software solutions, we have developed common software design tools that support the full range of integrated circuit products. We believe that automation and ease of design are significant competitive factors in the PLD segment.

Several companies, both large and small, have introduced products that compete with ours or have announced their intention to enter the PLD segment. Some of our competitors may possess innovative technology, which could prove superior to our technology in certain applications. In addition, we anticipate potential competition from suppliers of logic products based on new technologies. Some of our current or potential competitors have substantially greater financial, manufacturing, marketing and technical resources than we do. This additional competition could adversely affect our financial condition and results of operations.

We could also face competition from our licensees. Under a license from us, Lucent Technologies has rights to manufacture and market our XC3000 FPGA products and also employ that technology to provide additional high density FPGA products. Seiko Epson has rights to manufacture some of our products and market them in Japan and Europe, but is not currently doing so. We granted a license to use certain of our patents to Advanced Micro Devices (AMD). AMD produced certain programmable logic devices under that license through its wholly owned subsidiary, Vantis. In June 1999, AMD sold the Vantis subsidiary to Lattice Semiconductor Corporation.

Executive Officers of the Registrant

Certain information regarding each of Xilinx's executive officers is set forth below:

NAME	AGE	POSITION	OFFICER SINCE
Willem P. Roelandts	56	President and Chief Executive Officer	1996
Kris Chellam	50	Senior Vice President, Finance and Chief Financial Officer	1998
Steven Haynes	50	Vice President, Worldwide Sales	1998
Randy Ong	51	Vice President, Worldwide Operations	2000
Dennis Segers	48	Senior Vice President and General Manager of Advanced Products Group	1995
Richard W. Sevcik	53	Senior Vice President, IP, Services and Software Group	1997
Sandeep S. Vij	35	Vice President, Marketing and General Manager of General Products Division	1996
Evert A. Wolsheimer	46	Vice President, and General Manager of CPLD Division	2000

There are no family relationships among the executive officers of the Company. On the Board of Directors, Mr. Vonderschmitt, Chairman of the Board, is the brother-in-law of Mr. Sanda, Director.

Willem P. "Wim" Roelandts joined the Company in January 1996 as Chief Executive Officer and a member of the Company's Board of Directors. In April 1996, he was appointed to the additional position of President of the Company. Prior to joining the Company, he served at Hewlett-Packard Company, a computer manufacturer, as Senior Vice President and General Manager of Computer Systems Organizations from August 1992 through January 1996 and as Vice President and General Manager of the Network Systems Group from December 1990 through August 1992.

Kris Chellam joined the Company in July 1998 as Senior Vice President, Finance and Chief Financial Officer. Prior to joining the Company, he served at Atmel Corporation as Senior Vice President and General Manager of a product group from March to July 1998 and as Vice President, Finance and Administration, and Chief Financial Officer from September 1991 through March 1998. Mr. Chellam also serves as a director of At Road Inc.

Steven Haynes joined the Company in 1987 as the Regional Sales Manager of the Northeast region, was promoted to Area Sales Director in 1988, and was appointed Vice President, North American Sales in 1995. In November 1998, he was promoted and now holds the position of Vice President, Worldwide Sales.

Randy Ong joined the Company in 1990 as Senior Staff Engineer, and was promoted to Vice President of Worldwide Operations in 1997. He has overall responsibility for manufacturing, quality assurance, testing, reliability, and package development for Xilinx programmable logic devices. He also oversees strategic management of the Company's semiconductor foundry partners. He earned his bachelor's and master's degrees in electrical engineering at the University of California, Berkeley.

Dennis Segers joined the Company in January 1994 as Director of Strategic Products and was promoted to Vice President and General Manager in November 1995. In April 1998, he was appointed Senior Vice President, and General Manager of the Advanced Products Group. Mr. Segers is also a member of the Company's Board of Directors.

Richard W. Sevcik joined the Company in April 1997 as Senior Vice President, IP, Services and Software. He was at Hewlett-Packard Company for 10 years where, from 1994 through 1996, he served as Group General Manager of the company's Systems Technology Group and oversaw five divisions involved with product development for servers, workstations, operating systems, microprocessors, networking and security. In 1995 he was named Vice President. From 1992 to 1994, he served as Group General Manager of Computer Systems and Servers and was responsible for four divisions. Mr. Sevcik is also a member of the Company's Board of Directors.

Sandeep S. Vij joined the Company in April 1996 as Director, FPGA Marketing and was promoted to Vice President, Marketing in October 1996. In October 1997, he was appointed to the additional position of General Manager of the General Products Division. From 1990 until April 1996, he served at Altera Corporation, a semiconductor manufacturer, where he most recently served as the Product Marketing Manager of High Volume FPGAs.

Evert A. Wolsheimer joined the Company in 1991 as Vice President, Product Technology, with responsibility for process technology, wafer foundry, assembly, reliability, and product engineering. He was promoted to Vice President and General Manager of the CPLD Division in 1997. He has served on the Board of Directors of the Fabless Semiconductor Association (FSA) since 1997. Dr. Wolsheimer received his Ph.D. in Electrical Engineering from Delft University of Technology, The Netherlands.

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Item 2. Properties

Our corporate offices, which include the administrative, sales, customer support, marketing, research and development and final testing groups are located in San Jose, California. The site includes adjacent buildings providing 588,000 square feet of space which we own.

In addition, we have a 100,000 square foot administrative, research and development and final testing facility in the metropolitan area of Dublin, Ireland, a 60,000 square foot facility in Boulder, Colorado, and a 45,000 square foot facility in Albuquerque, New Mexico. The Irish facility is being primarily used to service our customer base outside of North America. The Boulder facility is the primary location for our software efforts in the areas of research and development, manufacturing and quality control while the New Mexico facility is being used for the development of our CoolRunner CPLD product. Additionally, we own a 59-acre parcel of land located in Longmont, Colorado, near our current Boulder facility. Groundbreaking to develop a new 130,000 square foot facility in Longmont was started in March 2000 and expected to be ready in September 2001. We also purchased another facility (200,000 sq. ft.) and 40 acres of land adjacent to the Longmont facility for the future expansion. The expansion of our Irish facility includes an additional 500,000 square feet of building and manufacturing space. The first phase of 100,000 square feet started in July 2000. In February 2001, we announced the addition of approximately 128,000 square feet expansion to our current facility in Dublin, Ireland to be constructed over a one-year period. This facility is currently under construction and it is our plan to complete the facility expansion by March 2002. We purchased 87 acres of land in San Jose, California, near our corporate facility in February 2000. Plans for infrastructure and the future development of this land have not been finalized. In September 2000, we purchased office buildings in San Jose due to the rapid growth of the Company. As of this time, the building is still being remodeled and expected to be ready for occupancy in fiscal 2002. We also lease, on a short-term basis, office facilities for our new acquired subsidiary, RocketChips, in Ames, Iowa, Minneapolis, Minnesota, and Austin, Texas.

We also maintain North American sales offices in various locations which include the metropolitan areas of Atlanta, Chicago, Denver, Dallas, Los Angeles, Minneapolis, Philadelphia, Raleigh, and San Jose as well as international sales offices located in the metropolitan areas of London, Munich, Paris, Stockholm, Milan, Brussels, Tel Aviv, Tokyo, Osaka, Taipei, Seoul, Hong Kong, and Shanghai.

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Item 3. Legal Proceedings

On June 7, 1993, we filed suit against Altera Corporation (Altera) in the United States District Court for the Northern District of California for infringement of certain of our patents. Subsequently, Altera filed suit against Xilinx, alleging that certain of our products infringe certain Altera patents. As a result of certain motions and rulings in the case, Altera is left with one claim against Xilinx, which remains the subject of a Company motion for summary judgment. A ruling on this motion is pending. If the remaining claim against Xilinx survives the motion for summary judgment, it will be decided at a trial, which is unscheduled at this point. The Court's rulings also dismissed certain claims by us, leaving intact claims of infringement by Altera under two Company patents. The remaining claims against Altera were decided at a trial which began on October 18, 2000. On November 17, 2000, a federal jury found that the two Company patents in the case were valid and that Altera infringed both patents. On May 10, 2001, the trial judge overturned the jury verdict, by granting Altera's motion to enter Judgment as a Matter of Law. The judge found that the Altera Flex 8000 product does not infringe one of the two Company patents, and that the other Company patent is invalid. The Company has filed its notice of appeal to reinstate the jury verdict, although no timetable for appeal has been set.

On April 20, 1995, Altera filed an additional suit against Xilinx in the Federal District Court in Delaware, alleging that our XC5200 family infringes an Altera patent. We answered the Delaware suit denying that the XC5200 family infringes the patent in suit, asserting certain affirmative defenses and counterclaiming that the Altera Max 9000 family infringes certain of our patents. The Delaware suit was transferred to the United States District Court for the Northern District of California.

On July 22, 1998, Altera and Joseph Ward, a former Xilinx employee, filed suit against Xilinx in Superior Court in Santa Clara County, California, arising out of our efforts to prevent disclosure of certain Company confidential information. Altera's suit requests declaratory relief and claims Xilinx engages in unfair business practices and interference with contractual relations. On September 10, 1998 we filed cross claims against Altera and Ward for unfair competition and breach of contract, among other claims, in the California action. On October 20, 1998, Altera and Ward filed crossclaims against Xilinx for malicious prosecution of civil action and defamation. On September 15, 1999, the Court dismissed all of our claims against Altera and Mr. Ward, finding that we were unable to show any damages we suffered as a result of any actions by Mr. Ward. On May 24, 2001, the Court dismissed all of Altera's claims against the Company leaving only Mr. Ward's claims of defamation against the Company.

On May 31, 2000, Altera filed an additional suit against Xilinx in the Federal District Court for the Northern District of California, alleging that certain Xilinx products, including our Virtex FPGAs, infringe three Altera patents. Altera's suit requests unspecified monetary damages as well as issuance of an injunction to prevent Xilinx from selling allegedly infringing parts. Xilinx has filed an amended answer and countercomplaint denying the allegations and alleging that the Altera patents are invalid and unenforceable because Altera engaged in inequitable conduct in acquiring the asserted patents. The counterclaim also alleges that Altera is infringing three additional Company patents. A claims construction hearing to determine the interpretation of Altera's patent claims was held on April 26 and 27, 2001. No decision has been rendered by the judge.

On November 16, 2000, we requested that the International Trade Commission investigate alleged infringements by Altera of three Company patents, and if so, to bar Altera from importing or selling such products into the United States. On December 18, 2000, the International Trade Commission decided to investigate our claims against Altera. A hearing has been set for June 25, 2001.

On March 9, 2001, the ITC at the request of Altera initiated an investigation against Xilinx based on two additional Altera patents. The matter has been assigned to Judge Harris, the same administrative law judge handling the ITC action by Xilinx against Altera. A hearing has been set for September 24, 2001.

The ultimate outcome of these matters cannot be determined at this time. Management believes that it has meritorious defenses to such claims and is defending them vigorously. The foregoing is a forward-looking statement subject to risks and uncertainties, and the future outcome of these matters could differ materially due to the uncertain nature of each legal proceeding and because most of the lawsuits are still in the pre-trial stages.

There are no other pending legal proceedings of a material nature to which we are a party or of which any of our property is the subject. Other than the petition filed by the Company with the Tax Court on March 26, 2001 (See Management's Discussion and Analysis of Financial Condition and Results of Operations, Provision for Income Taxes), we know of no legal proceedings contemplated by any governmental authority or agency.

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Item 4. Submission of Matters to a Vote of Security Holders

No matters were submitted to a vote of security holders during the fourth quarter of the fiscal year covered by this report.

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Item 5. Market for the Registrant's Common Equity and Related Stockholder Matters

Xilinx's Common Stock is listed on the NASDAQ National Market System under the symbol XLNX. As of March 31, 2001, there were approximately 1,515 shareholders of record. Since many holders' shares are listed under their brokerage firms' names, the actual number of shareholders is estimated by the Company to be approximately 195,000.

	FISCAL YEAR 2001		FISCAL YEAR 2000	
	HIGH	LOW	HIGH	LOW
First Quarter	$ 97.94	$ 55.75	$ 29.28	$ 20.28
Second Quarter	96.63	69.88	37.53	29.28
Third Quarter	89.63	39.00	47.81	33.25
Fourth Quarter	57.63	35.13	86.81	40.81

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Item 6. Selected Financial Data

Consolidated Statements of Income Data

(IN THOUSANDS EXCEPT PER SHARE AMOUNTS)	YEARS ENDED MARCH 31, 2001(4)	2000(3)	1999(2)	1998	1997(1)
Net revenues	$ 1,659,358	$ 1,020,993	$ 661,983	$ 613,593	$ 568,143
Operating income	384,053	322,192	181,974	173,868	159,061
Income before equity in joint venture and cumulative effect of change in accounting principle	61,103	1,024,272	189,399	180,596	165,758
Provision for income taxes	25,845	378,006	54,925	56,728	55,382
Net income	35,258	652,450	102,592	126,587	110,376
Net income per share:					
Basic	$ 0.11	$ 2.06	$ 0.35	$ 0.43	$ 0.38
Diluted	$ 0.10	$ 1.90	$ 0.33	$ 0.40	$ 0.35
Shares used in per share calculations:					
Basic	328,196	316,724	292,843	294,963	291,264
Diluted	353,345	343,479	308,620	320,041	318,700
Pro forma amounts with the change in accounting principle related to revenue recognition applied retroactively: (unaudited)					
Net revenues	–	–	$ 661,983	$ 598,065	$ 568,173
Net income	–	–	129,238	118,987	110,391
Net income per share:					
Basic	–	–	$ 0.44	$ 0.40	$ 0.38
Diluted	–	–	$ 0.42	$ 0.37	$ 0.35

(1) After write-off of discontinued product family of $5,000, $0.02 per basic and diluted shares net of tax.
(2) Net income includes a charge of $26,646 for the cumulative effect of change in accounting principle.
(3) Net income includes pre-tax capital gain of $674,728 ($398,089 net of tax) from UMC/USIC merger.
(4) Net income includes pre-tax write down loss of $362,124 on UMC investment.

Consolidated Balance Sheet Data

(IN THOUSANDS)	MARCH 31, 2001	2000	1999	1998	1997
Working capital	$ 751,469	$ 796,213	$ 490,512	$ 474,567	$ 504,302
Total assets	2,502,196	2,348,639	1,070,248	941,238	847,693
Long-term debt	–	–	–	250,000	250,000
Stockholders' equity	1,918,316	1,776,655	879,318	550,175	490,680

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Item 7. Management's Discussion and Analysis of Financial Condition and Results of Operations

Cautionary Statement

The statements in this Management's Discussion and Analysis that are forward looking involve numerous risks and uncertainties and are based on current expectations. You should not place undue reliance on these forward-looking statements. Our actual results could differ materially from those anticipated in these forward-looking statements for many reasons, including those risks discussed under "Factors Affecting Future Operating Results" and elsewhere in this document. Forward looking statements can often be identified by the use of forward looking words, such as "may," "will," "could," "should," "expect," "believe," "anticipate," "estimate," "continue," "plan," "intend," "project," or other similar words.

Nature of Operations

Xilinx, Inc. (Xilinx or the Company) designs, develops and markets complete programmable logic solutions, including advanced integrated circuits (ICs), software design tools, predefined system functions delivered as cores of logic, design services, customer training, and field engineering support. Our programmable logic ICs include field programmable gate arrays (FPGAs) and complex programmable logic devices (CPLDs). These components are standard ICs programmed by our customers to perform desired logic operations. Our products are designed to provide high integration and quick time-to-market for electronic equipment manufacturers primarily in communications, storage, servers, instrumentation, industrial, and other markets. We market our products throughout the world through a direct sales organization, direct sales to original equipment manufacturers by independent sales representative firms, sales through franchised domestic and foreign distributors.

Results of Operations

Net Revenue

(IN THOUSANDS)	2001	CHANGE	2000	CHANGE	1999
Net revenues	$1,659,358	62.5%	$1,020,993	54.2%	$661,983

Xilinx's net revenue increased 62.5% in fiscal 2001 compared to fiscal 2000. The increase was primarily due to the significant growth in Spartan and Virtex product lines. Net revenue growth slowed substantially in the fourth quarter of fiscal 2001 due to decelerating bookings and order cancellations resulting from asoftening economy and increased inventory levels experienced by a broad base of customers. 54.2% increase in fiscal 2000 over 1999 was primarily due to the significant growth in XC4000XL, XC4000XLA, XC9500, Spartan™, and Virtex product lines, which was partially offset by decreased revenues in our mature XC4000 family.

We classify our product offerings into four categories by semiconductor manufacturing process technology. These four product categories are adjusted on a regular basis to accommodate advances in our process technology. **Advanced products** include our newest technologies manufactured on 0.25-micron and smaller processes, which include the XC4000XV, XC4000XLA, Spartan XL™, Spartan-II™, Virtex™, Virtex-E™ and Virtex II product lines. Advanced products represented 51.0% and 26.7% of total revenues in fiscal 2001 and 2000. The significant increases in revenues of advanced products were due to the introduction and strong market acceptance of Virtex-E and Spartan II products. **Mainstream products** are currently manufactured on 0.35 and 0.5-micron technologies and include the XC4000E, XC4000EX, XC4000XL, XC5200, XC9500, XC9500XL, Spartan™ and CoolRunner product lines. Mainstream products represented 35.3% of total revenues in fiscal 2001 and 52.6% in fiscal 2000. Mainstream products saw the heaviest revenue decline in the 4000XL and 9500 product families due to the combination of the softening economy, excess inventory in the channel, and customer's migration to newer production offerings. **Base products** consist of our mature product families that are currently manufactured on technologies of 0.6-micron and older; this includes the XC2000, XC3000, XC3100, and XC4000 families. Base products represented 6.3% of total revenues in fiscal 2001, as compared to 12.3% in fiscal 2000. Our **Support products** make up the remainder of our product offerings and include configuration solutions, serial proms, HardWire, software and support. Support products represented 7.4% and 8.4% of total revenues in fiscal 2001 and 2000, respectively. No end customer accounted for more than 10% of revenues in fiscal 2001, 2000 or 1999. The revenue by technology for the years ended March 31, 2001, 2000 and 1999 was as follows:

(IN MILLIONS)	2001	%	2000	%	1999	%
Advanced products	$ 845.8	51.0	$ 272.8	26.7	$ 20.4	3.1
Mainstream products	585.6	35.3	537.0	52.6	417.1	63.0
Base products	104.5	6.3	125.5	12.3	146.8	22.2
Support products	123.5	7.4	85.7	8.4	77.7	11.7
Total revenue	$1,659.4	100.0	$1,021.0	100.0	$662.0	100.0

In order to compete effectively, we pass manufacturing cost reductions to our customers in the form of reduced prices to the extent that we can maintain acceptable returns. Price erosion has been common in the semiconductor industry, as advances in both product architecture and manufacturing process technology have permitted continual reductions in unit cost. We have historically been able to offset much of the revenue declines of our mature technologies with increased revenues from newer technologies, although no assurance can be given that we can continue to do so in the future.

The revenue by geography for the years ended March 31, 2001, 2000, and 1999 was as follows:

(IN MILLIONS)	2001	%	2000	%	1999	%
North America	$1,028.2	62	$ 681.1	66.7	$447.2	67.5
Europe	334	20.1	201.8	19.8	139.8	21.1
Japan	163.6	9.9	82.6	8.1	47.5	7.2
Asia Pacific/Rest of World	133.6	8.0	55.6	5.4	27.5	4.2
Total revenue	$1,659.4	100.0	$1,021.0	100.0	$662.0	100.0

International revenues represented approximately 38%, 33%, and 32% of total revenues for fiscal years 2001, 2000, and 1999, respectively. Europe, Japan, and Asia Pacific/Rest of World experienced revenue growth in fiscal 2001 as compared to fiscal 2000 due to wider adoption of our new products in consumer and telecommunication applications.

During the fourth quarter of fiscal 1999, we changed our accounting method for recognizing revenue on all shipments to international distributors. The change was made retroactive to the beginning of fiscal 1999. While we previously deferred revenue on shipments to domestic distributors until the products were sold to the end user, we recognized revenue upon shipment to international distributors, net of appropriate reserves for returns and allowances. Following the accounting change, revenue recognition on shipments to distributors worldwide is deferred until the products are sold to the end customer. We believe that deferral of revenue on shipments to distributors until the product is shipped by the distributor to an end customer is a more meaningful measurement of results of operations, and is consistent with industry practice. Accordingly, it is a preferable method of accounting for revenue. The cumulative effect of the change in accounting method for prior years was a charge of $26.6 million, net of $12.0 million in taxes, or $0.09 net income per diluted share.

Gross Margin

(IN THOUSANDS)	2001	CHANGE	2000	CHANGE	1999
Gross margin	$979,956	53.9%	$636,955	55.1%	$410,717
Percentage of net revenues	59.1%		62.4%		62.0%

During fiscal 2001, our gross margin percentage decreased from the prior year primarily due to the write-down for inventory in excess of the demand and backlog due to a slow down in business during the fourth quarter of fiscal 2001. In addition, the gross margin percentage decreased from the prior year due to lower margin new products such as Spartan II and Virtex-E and the decline in revenue of our older more profitable product families. During fiscal 2000, our gross margin percentage increased slightly from the prior year as efficiencies from increased production volumes resulted in decreased costs as a percentage of revenue.

Research and Development

(IN THOUSANDS)	2001	CHANGE	2000	CHANGE	1999
Research and development	$213,195	72.5%	$123,584	36.0%	$90,893
Percentage of net revenues	12.8%		12.1%		13.7%

Research and development expenditures were $213.2 million ($208.7 million excluding RocketChips deferred stock compensation. See Note 13 of Notes to Consolidated Financial Statements) and $123.6 million for fiscal year 2001 and 2000, respectively. We increased our expenditures in research and development as we have done each year during our seventeen-year history. The increase in research and development expenditures from fiscal 2000 to 2001 was related to designing new complex and high density devices, mask and wafer purchases, development of advanced process technologies, software development, increased labor-related costs associated with the development of new products along with increased labor costs associated with the acquisition of RocketChips. (See Note 13 of Notes to Consolidated Financial Statements.) The increase in research and development expenditures from fiscal 1999 to 2000 was related to designing new complex and high density devices, wafer purchases, development of advanced process technologies using 0.22-micron and 0.18-micron technologies, software development, increased labor-related costs, along with increased costs associated with the acquisition of the CoolRunner CPLD business. We remain committed to a significant level of research and development effort in order to extend our technology leadership in the programmable logic marketplace. Through March 31, 2001, we have received over 545 issued U.S. patents and we maintain an active program of filing for additional patents in the areas of circuit design and software.

Sales, General and Administrative

(IN THOUSANDS)	2001	CHANGE	2000	CHANGE	1999
Sales, general and administrative	$274,093	46.9%	$186,619	39.0%	$134,250
Percentage of net revenues	16.5%		18.3%		20.3%

Selling, general and administrative expenses for the year ended March 31, 2001 were $274.1 million, or 16.5% of net revenues, compared to $186.6 million, or 18.3% of net revenues in the fiscal 2000 and $134.3 million, or 20.3% of net revenues in the fiscal 1999. Although total selling, general and administrative spending increased, they decreased as a percentage of net revenues because of strong revenue growth and operational efficiencies. The 46.9% increase in sales, general and administrative expenses in fiscal 2001 was primarily attributable to increased personnel and facilities expenses, increased advertising and promotional

expenditures, increased outside sales commissions and sales incentives on higher revenues and legal expenses. Sales, general and administrative expenses increased 39.0% in fiscal 2000 over 1999 due to increased personnel and facilities expenses, increased marketing expenses and higher commission and incentive expenses associated with increased sales. We remain committed to controlling administrative expenses. However, the timing and extent of future legal costs associated with the ongoing enforcement of our intellectual property rights are not readily predictable and may increase in the future.

Write-Off of In-Process Technology

In connection with the acquisition of RocketChips in fiscal 2001, approximately $90.7 million of in-process research and development costs were incurred. In fiscal 2000, in connection with the acquisition of Philips Semiconductors' line of low-power complex programmable logic devices (CPLDs), approximately $4.6 million was incurred for the research and development project in process and in fiscal 1999 in the acquisition of MI Acquisition LLP, approximately $3.6 million was related to research and development in process. The projects identified as in-process will require additional effort in order to establish technological feasibility. These projects have identifiable technological risk factors that indicate that even though successful completion is expected, it is not assured. If an identified project is not successfully completed there is no alternative future use for the project and the expected future income will not be realized. The acquired in-process technology represents the appraised value of technologies in the development stage that had not yet reached technological feasibility and do not have alternative future uses.

To determine the value of the in-process research and development, the expected future cash flow attributable to the in-process technology was discounted, taking into account the percentage of completion, utilization of preexisting "core" technology, risks related to the characteristics and applications of the technology, existing and future markets, and technological risk associated with completing the development of the technology. We immediately expense this non-recurring charge in the period of acquisition. (See Note 13 of Notes to Consolidated Financial Statements.)

Capital Gain from Merger of USIC with UMC

In January 2000 United Silicon Inc. (USIC) was merged into United Microelectronics Corp (UMC) and our equity position in USIC was converted into shares of UMC which are publicly traded on the Taiwan Stock Exchange. We recognized a non-cash gain of $674.7 million ($398.1 million net of taxes) in fiscal 2000 as a result of the merger of USIC with UMC. The gain represents the appreciation of our investment in USIC. As a result of this merger, we received approximately 222 million UMC shares, which represent approximately 2% of the combined UMC Group. In July 2000, we received a 20% stock dividend which increased our investment holdings in UMC to approximately 266 million shares. We retain equivalent wafer capacity rights in UMC as we previously had in USIC, as long as we retain a defined percentage of our shares of UMC common stock. If our holdings fall below that percentage, our wafer capacity rights would be prorated by the UMC shares we hold.

Due to restrictions imposed by UMC and the Taiwan Stock Exchange, the majority of our UMC shares could not be sold until July 2000. These regulatory restrictions will gradually expire between July 2000 and January 2004.

Write-Down on UMC Investment Valuation

Due to the current weakness in the semiconductor industry, the value of our UMC shares declined to $430.9 million as of March 31, 2001. The downturn in the semiconductor industry and the economy in general, appears to be more severe than previously anticipated, and there is a great deal of uncertainty regarding when the semiconductor industry will recover from this down cycle. Because of the continued downturn in the economy, we believe that the decline in the market value of our investment in UMC as of March 31, 2001, was other than temporary as defined by accounting principles generally accepted in the United States. In the fourth quarter of fiscal 2001 we recognized a pre-tax loss of $362.1 million. If the value our UMC shares declines further, we may be required to record additional losses. In addition, in future periods, we may recognize a gain or loss if we sell our UMC shares due to fluctuations in the market value of UMC stock.

Interest and Other Income, net

(IN THOUSANDS)	2001	CHANGE	2000	CHANGE	1999
Interest income and other income, net	$39,174	43.2%	$27,352	268.4%	$7,425
Percentage of net revenues	2.4%		2.7%		1.1%

Interest and other income was $39.2 million, or 2.4% of net revenues in fiscal 2001 compared to $27.4 million, or 2.7% of net revenues in fiscal 2000 and $7.4 million, or 1.1% of net revenues in fiscal 1999. For fiscal 2001, interest and other income included a pre-tax gain on our investment in Nuron LLC of $4.5 million due to Nuron being purchased by a public company. Excluding the Nuron LLC gain, net interest and other income was $34.6 million, or 2.1% of sales. Excluding the Nuron LLC gain, the dollar increase from fiscal year 2000 to 2001 was primarily due to an increase in the interest income related to higher investment balances and higher interest rates offset by foreign exchange losses due to the weaker Japanese Yen in fiscal 2001 compared to fiscal 2000.

The 268% increase in interest and other income in fiscal 2000 from fiscal 1999 was primarily due to the $11.2 million decrease in interest expense related to the redemption in February 1999 of our previously outstanding convertible notes in February 1999 and increased interest income on higher average cash and investment balances. The amount of net interest and other income in the future will continue to be impacted by the level of our average cash and investment balances, prevailing interest rates, the balance of any debt outstanding, and foreign currency exchange rates.

Provision for Income Taxes

(IN THOUSANDS)	2001	CHANGE	2000	CHANGE	1999
Provision for taxes on income	$25,845	(93.2%)	$378,006	588.2%	$54,925
Effective tax rate	42.3%		36.9%		29.0%

The effective tax rate in fiscal 2001 is higher than fiscal 2000 principally due to in-process research and development charges with no corresponding tax benefit to the company. The effective tax rate in fiscal 2000 was higher than fiscal 1999 principally due to taxes of $277 million on a $675 million gain realized on the UMC/USIC merger, which significantly offset tax benefits associated with tax exempt interest and foreign earnings at lower tax rates which generally reduce our effective tax rate. (See Note 10 of Notes to Consolidated Financial Statements.)

On December 28, 2000, the Internal Revenue Service issued a statutory notice of deficiency reflecting proposed audit adjustments

for fiscal years 1996, 1997, and 1998. We filed a petition with the Tax Court on March 26, 2001 contesting this notice of deficiency. We believe we have meritorious defenses to the proposed adjustments and sufficient taxes have been provided.

Joint Venture Equity Converted to UMC Shares

We recorded our proportional ownership of the net income (loss) of USIC, a wafer fabrication joint venture located in Taiwan, as joint venture equity income (loss) prior to the merger of USIC and UMC. In fiscal 2000, income was generated as USIC began to realize volume wafer production and shipments. The fiscal 1999 net loss was a result of the continued ramp up in production of the wafer fabrication facility.

As a result of the conversion of our equity position in USIC to shares of UMC in January 2000, as discussed above, we no longer record joint venture equity income.

Inflation

To date, the effects of inflation upon our financial results have not been significant. We cannot assure, however, inflation will not affect us materially in the future.

Financial Condition, Liquidity and Capital Resources

We have used a combination of equity and debt financing and cash flow from operations to support on-going business activities, acquiring critical technologies, and making investments in complementary technologies, purchase facilities and capital equipment, and finance inventory and accounts receivable. Additionally, our investment in UMC is available for future sale, subject to restrictions.

Cash, Cash Equivalents and Short-term Investments

During fiscal 2001, we generated cash flow of $377.3 million from operating activities, $44.7 million from investing activities, and consumed $298.8 million from financing activities. Investing activities during fiscal 2001 included $263.1 million in net proceeds from sales and purchases of investments, $4 million cash obtained from acquisition of Rocketchips, Inc, offset by $222.7 million expenditures for property, plant and equipment. Financing activities during fiscal year 2001 included an increase of $104.0 million from issuance of common stocks and sales of put warrants, offset by $402.8 million of stock buyback.

During fiscal 2000, we generated cash flow of $341.1 million from operating activities and $89.1 million from financing activities, offset by $398.2 million of cash used for investing activities. Investing activities during fiscal 2000 included $231.7 million in net purchases of investments, $143.7 million expenditures for property, plant and equipment, and $22.8 million for the purchase of Philips' CPLD business. Financing activities during 2000 included $84.3 million in proceeds from sales of common stock under employee option and stock purchase plans and $10.0 million from sales of put warrants partially offset by $5.3 million of stock buyback.

Receivables

Receivables increased 27.9 % from $135.0 million at the end of fiscal 2000 to $172.8 million at the end of fiscal 2001. The increase was primarily attributable to the increased level of sales.

Inventories

Inventories increased from $131.3 million at March 2000 to $342.5 million at March 2001 due to the increased level of sales. In the fourth quarter of fiscal 2001, we wrote down inventory due to a decrease in forecasted demand. Given the volatility of the market and the obsolescence in technology and shorter product life cycles, we write down inventories to net realizable value based on backlog and forecasted demand. However, backlog is subject to revisions, cancellations and rescheduling. Actual demand may differ from forecasted demand and such difference may have a material effect on our financial position and result of operations.

We attempt to maintain sufficient levels of inventory in various product, package and speed configurations to meet forecasted customer demand. On the other hand, we also wish to minimize the handling costs associated with maintaining higher inventory levels and to fully realize the opportunities for cost reductions associated with architecture and manufacturing process advancements. We continually strive to balance these two objectives to provide excellent customer response at a competitive cost.

Property, Plant and Equipment

During 2001, we invested $222.7 million in property and equipment compared to $143.7 million in 2000. Primary investments in fiscal 2001 were for land and building purchases, software and semiconductor design tools, test and manufacturing equipment at each of our manufacturing and test locations, and workstations and network infrastructure to support the increased level of business.

Current Liabilities

Current liabilities increased from $244.7 million at the end of fiscal 2000 to $350.4 million at the end of fiscal 2001. The increase was primarily attributable to the increase in accounts payable and deferred income on shipments to distributors. The increase in accounts payable was a result of business expansion and the increase in deferred income on shipments to distributors was due to increased inventory build up at distributors, due to the higher sales in fiscal 2001 compared to fiscal 2000.

Long-term Debt and Lines of Credit

In fiscal 1999, we converted in full $250.0 million 5_% Convertible Subordinated Notes due 2002 for a total of 19.6 million shares of common stock at a price of $12.75 per share. We have credit facilities for $6.2 million to meet occasional working capital requirements for our Ireland manufacturing facility. The other $40.0 million revolving credit agreement expired on March 26, 2001 and we decided not to extend this line of credit. At March 31, 2000, no borrowings were outstanding under the lines of credit. (See Note 5 of Notes to Consolidated Financial Statements.)

Stockholders' Equity

Stockholders' equity grew by 8% in fiscal 2001 to $1,918.3 million. The increase of $141.7 million was attributable to $35.3 million in net income, $241.8 million related to the issuance of common stock from employee stock plans and the tax benefit from stock options, $268.6 million from the stock issuance in connection with RocketChips acquisition (See Note 3 of Notes to Consolidated

Financial Statements), and $22.2 million related to the sale of put warrants. The increases were offset by the $402.8 million used to acquire treasury stock and $23.4 million from unrealized loss on available for sale securities and our cumulative translation adjustment.

Summary of Liquidity

We anticipate that existing sources of liquidity and cash flow from operations will be sufficient to satisfy our cash needs for the foreseeable future. However, the risk factors discussed below could affect our cash positions adversely. We will continue to evaluate opportunities for investments to obtain additional wafer capacity, procurement of additional capital equipment and facilities, development of new products, and potential acquisitions of technologies or businesses that could complement our business. We may use available cash or other sources of funding for such purposes.

Factors Affecting Future Operating Results

The semiconductor industry is characterized by rapid technological change, intense competition and cyclical market patterns. Cyclical market patterns are characterized by several factors, including:

- reduced product demand;
- limited visibility of demand for products beyond three months;
- accelerated erosion of average selling prices;
- tight capacity availability;
- shortages of other electronic components;
- excess inventory within the supply chain; and
- overbuilding of OEM products, including communication infrastructure.

Our results of operations are affected by several factors. These factors include general economic conditions, conditions specific to technology companies and to the semiconductor industry in particular, decreases in average selling prices over the life of particular products and the timing of new product introductions (by us, our competitors and others.) In addition, our results of operations are affected by the ability to manufacture sufficient quantities of a given product in a timely manner, the timely implementation of new manufacturing technologies, the ability to safeguard patents and intellectual property from competitors, the impact of new technologies which result in rapid escalation of demand for some products in the face of equally steep declines in demand for others, and the inability to predict the success of our customers' products in their markets. Market demand for our products, particularly for those most recently introduced, can be difficult to predict, especially in light of customers' demands to shorten product lead times and minimize inventory levels. Shortages of other electronic components could lead to customers canceling orders for our products due to the inability to complete their end system. Unpredictable market demand could lead to revenue volatility if we were unable to provide sufficient quantities of specified products or if our customers' reduced demand cause them to slow orders of our products. In addition, any difficulty in achieving targeted wafer production yields could adversely affect our financial condition and results of operations. We attempt to identify changes in market conditions as soon as possible; however, the dynamics of the market make prediction of and timely reaction to such events difficult. Due to these and other factors, our past results, including those described in this report, are much less reliable predictors of the future than with companies in many older, more stable and mature industries. Based on the factors noted herein, we may experience substantial period-to-period fluctuations in future operating results.

Our future success depends in a large part on the continued service of our key technical, sales, marketing and management personnel and on our ability to continue to attract and retain qualified employees. Particularly important are those highly skilled design, process, product, software and test engineers involved in the manufacture of existing products and the development of new products and processes. The competition for such personnel is intense, and the loss of key employees could have a material adverse effect on our financial condition and results of operations.

Sales and operations outside of the United States subject us to the risks associated with conducting business in foreign economic and regulatory environments. Our financial condition and results of operations could be adversely affected by unfavorable economic conditions in countries in which we do significant business and by changes in foreign currency exchange rates affecting those countries. For example, we have sales and operations in Asia Pacific and Japan. Past economic weakness in these markets adversely affected revenues, and such conditions may occur in the future. While the recent weakness of the Euro and Yen against the Dollar has had no material impact to our business, continued weakness could lead to adverse conditions from our European and Japanese customers. Customers may face reduced access to capital and exchange rate fluctuations may adversely affect their ability to purchase our products. In addition, our ability to sell at competitive prices may be diminished. Currency instability may increase credit risks as the weak currencies may impair our customers' ability to repay existing obligations. Any or all of these factors could adversely affect our financial condition and results of operations in the near future.

Our financial condition and results of operations are becoming increasingly dependent on the global economy. Any instability in worldwide economic environments could lead to a contraction of capital spending by our customers. Additional risks to us include government regulation of exports, imposition of tariffs and other potential trade barriers, reduced protection for intellectual property rights in some countries and generally longer receivable collection periods. Moreover, our financial condition and results of operations could be affected in the event of political conflicts in Taiwan where our main foundry partner, UMC, as well as a significant number of suppliers to the semiconductor industry, end-customers and contract manufacturers who provide manufacturing services worldwide, are located.

Our business is also subject to the risks associated with the imposition of legislation and regulations relating specifically to the import or export of semiconductor products. We cannot predict whether quotas, duties, taxes or other charges or restrictions will be imposed by the United States or other countries upon the import or export of our products in the future or what effect, if any, such actions would have on our financial condition and results of operations.

We do not manufacture our own silicon wafers. Presently, all of our wafers are manufactured by our foundry partners in Taiwan by UMC and in Japan by Seiko Epson Corp (Seiko). We depend on our foundry partners to deliver reliable silicon wafers, with acceptable yields, in a timely manner. If our foundry partners are unable to produce and deliver silicon wafers that meet our specifications, including acceptable yields, our results of operation could be adversely affected.

Our foundry partners in Taiwan and Japan and many of our operations in California are centered in areas that have been seismically active in the recent past. Should there be a major earthquake in our operating locations in the future, our operations, including our manufacturing activities, may be disrupted. This type of disruption could result in our inability to ship products in a timely manner, thereby materially adversely affecting our financial condition and results of operations.

Our headquarters in San Jose, California, performs design and test services for certain of the Company's products. These services

require the continuous use of electrical power and, at times of high usage, we are susceptible to the electrical power outages occurring in California. Any prolonged periods of electrical "blackouts" in California could have a material and adverse effect on our ability to perform design and test services at our headquarters.

The securities of many high technology companies have historically been subject to extreme price and volume fluctuations, which may adversely affect the market price of our common stock.

Dependence Upon Independent Manufacturers and Subcontractors

We do not manufacture the semiconductor wafers used for our products. During the past several years, most of our wafers have been manufactured by UMC and Seiko, with recent wafers also manufactured by USIC until its merger into UMC. We are dependent upon these suppliers and others to produce wafers with competitive performance and cost attributes which include transitioning to advanced manufacturing process technologies, producing wafers at acceptable yields and delivering them in a timely manner. While the timeliness, yield and quality of wafer deliveries have met our requirements to date, we cannot guarantee that our wafer suppliers will not experience future manufacturing problems, including delays in the realization of advanced manufacturing process technologies. Additionally, disruption of operations at these foundries for any reason, including natural disasters such as fires, floods, or earthquakes, as well as disruptions in access to adequate supplies of electricity, natural gas or water could cause delays in shipments of our products, and could have a material adverse effect on our results of operations. We are also dependent on subcontractors located in Asia to provide semiconductor assembly services. The more complex product design also requires more advanced assembling and packaging technology developed by our subcontractors. Any prolonged inability to obtain wafers or assembly services with competitive performance and cost attributes, adequate yields or timely delivery, or any other circumstance that would require us to seek alternative sources of supply, could delay shipments and have a material adverse effect on our financial condition and results of operations.

Our growth will depend in large part upon our ability to obtain additional wafer fabrication capacity and assembly services from suppliers that are cost competitive during a period of tight capacity availability. We consider various alternatives in order to secure additional wafer capacity. These alternatives include, without limitation, equity investments in, or loans, deposits, or other financial commitments to independent wafer manufacturers. We also consider the use of contracts which commit us to purchase specified quantities of wafers over extended periods. We are currently able to obtain wafers from existing suppliers in a timely manner. However, at times we have been unable, and may in the future be unable, to fully satisfy customer demand because of production constraints, including the ability of suppliers and subcontractors to provide materials and services to satisfy customer delivery dates, as well as our ability to process products for shipment. In addition, a significant increase in general industry demand or any interruption of supply could reduce our supply of wafers or increase our cost of such wafers. These events could have a material adverse effect on our financial condition and results of operations.

Dependence on New Products

Our success depends in large part on our ability to develop and introduce new products which address customer requirements and compete effectively on the basis of price, density, functionality, and performance. The success of new product introductions is dependent upon several factors, including:

- timely completion of new product designs;
- ability to utilize advanced manufacturing process technologies including advanced mask making capability;
- achieving acceptable yields;
- ability to obtain advanced packaging;
- availability of supporting software design tools;
- utilization of predefined cores of logic;
- market acceptance; and
- successful deployment of systems by our customers.

We cannot assure that our product development efforts will be successful or that our new products will achieve market acceptance. Revenues relating to our mature products are expected to decline in the future. As a result, we will be increasingly dependent on revenues derived from newer products along with cost reductions on current products. We rely primarily on obtaining yield improvements and corresponding cost reductions in the manufacture of existing products and on introducing new products which incorporate advanced features and other price/performance factors that enable us to increase revenues while maintaining consistent margins. To the extent that such cost reductions and new product introductions do not occur in a timely manner, or to the extent that our products do not achieve market acceptance at prices with higher margins, our financial condition and results of operations could be materially adversely affected.

Competition

See "competition" discussed in Item 1.

Intellectual Property

We rely upon patent, copyright, trade secret, mask work and trademark law to protect our intellectual property. We cannot assure that such intellectual property rights can be successfully asserted in the future or will not be invalidated, circumvented or challenged. From time to time, third parties, including our competitors, have asserted patent, copyright, and other intellectual property rights to technologies that are important to us. We cannot assure that third parties will not assert infringement claims against us in the future, that assertions by third parties will not result in costly litigation or that we would prevail in such litigation or be able to license any valid and infringed patents from third parties on commercially reasonable terms. Litigation, regardless of its outcome, could result in substantial costs and diversion of our resources. Any infringement claim or other litigation against us or by us could materially adversely affect our financial condition and results of operations. (See Part I — Other Information, Item 3 — Legal Proceedings for a discussion of litigation between Xilinx and Altera Corporation.)

Investment Company Act of 1940

The Investment Company Act of 1940 regulates mutual funds and closed-end investment companies that are traded on the public stock markets. In January 2000, as a result of USIC's merger with UMC (see Note 4 to Consolidated Financial Statements), we received approximately 222 million shares of UMC stock, which are publicly traded on the Taiwan Stock Exchange. (Our current holdings in UMC equal approximately 266 million shares as the result of a stock dividend in July 2000 - See Note 4 to Consolidated Financial Statements). We view this investment in UMC as an operating investment primarily intended to secure adequate wafer manufacturing capacity. Although from time to time we could be viewed as holding a larger portion of our assets in investment securities than is presumptively permitted by the 1940 Act for a company not registered as an investment company due to the success of our investments, in particular UMC, we believe we should not be considered an investment company under the Act. The

1940 Act, and rules issued under it, contain provisions and set forth principles that are designed to differentiate "true" operating companies from companies that may be considered to have sufficient investment company-like characteristics to require regulation by the 1940 Act. At this time, we believe that we qualify as an operating company under these provisions. In the future, however, our situation may change which might require us to seek an alternate solution such as exemptive or no-action relief from the SEC.

Euro Currency

Beginning in 1999, 11 member countries of the European Union established fixed conversion rates between their existing sovereign currencies and adopted the Euro as their common legal currency. During the three-year transition, the Euro will be available for non-cash transactions and legacy currencies will remain legal tender. We are continuing to assess the Euro's impact on our business. We are reviewing the ability of our accounting and information systems to handle the conversion, the ability of foreign banks to report on dual currencies, the legal and contractual implications of agreements, as well as reviewing our pricing strategies. We expect that any additional modifications to our operations and systems will be completed on a timely basis and do not believe the conversion will have a material adverse impact on our operations. However, we cannot assure that we will be able to successfully modify all systems and contracts to comply with Euro requirements.

Litigation

We are currently engaged in several legal matters. See "Legal Proceedings" in Part I.

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Item 7A. Quantitative and Qualitative Disclosures about Market Risk

Interest Rate Risk

Our exposure to interest rate risk relates primarily to our investment portfolio. Our primary aim with our investment portfolio is to invest available cash while preserving principal and meeting liquidity needs. The portfolio includes tax-advantaged municipal bonds, tax-advantaged auction rate preferred municipal bonds, commercial paper, and U.S. Treasury securities. In accordance with our investment policy, we place investments with high credit quality issuers and limit the amount of credit exposure to any one issuer. These securities are subject to interest rate risk and will decrease in value if market interest rates increase. A hypothetical 10% increase in interest rates would not materially affect the fair value of our available-for-sale securities.

Foreign Currency Risk

We enter into forward currency exchange contracts to reduce financial market risks. Our sales to Japanese customers are denominated in yen while our purchases of processed silicon wafers from Japanese foundries are primarily denominated in U.S. dollars. Gains and losses on foreign currency forward contracts that are designated and effective as hedges of anticipated transactions, for which a firm commitment has been attained, are deferred and included in the basis of the transaction in the same period that the underlying transactions are settled. Gains and losses on any instruments not meeting the above criteria would be recognized in income in the current period. A 15% adverse change in yen exchange rates based on historical average rate fluctuations would have had approximately a 1.85% adverse impact on revenue for the twelve months ended in fiscal years 2001. We are also sharing the yen exchange rate risk with some of our Japanese customers through risk sharing agreements. As we will continue to have a net yen exposure in the near future, we will continue to mitigate the exposure through yen hedging contracts. However, no currency forward contracts were outstanding for Japanese Yen as of March 31, 2001.

As we plan to expand our Ireland facility, we have four outstanding forward currency exchange contracts against Euro with Bank of America. Total value of contracts is US$10 million. The four contracts expire at various dates between May and September 2001. Since we will continue to have Euro currency exposure over the expansion period, we will continue to mitigate the exposure through Euro hedging contracts.

Our investments in several subsidiaries and in the UMC securities are recorded in currencies other than the U.S. dollar. As these foreign currency denominated investments are translated at each month end during consolidation, fluctuations of exchange rates between the foreign currency and the U.S. dollar increase or decrease the value of those investments. If permanent changes occur in exchange rates after an investment is made, the investment's value will increase or decrease accordingly. These fluctuations are recorded within stockholders' equity as a component of accumulated other comprehensive income. Also, as our subsidiaries maintain investments denominated in other than local currencies, exchange rate fluctuations will occur.

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Item 8. Financial Statements and Supplementary Data

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Consolidated Statements of Income

(IN THOUSANDS EXCEPT PER SHARE AMOUNTS)	YEARS ENDED MARCH 31, 2001	2000	1999
Net revenues	$ 1,659,358	$ 1,020,993	$ 661,983
Costs and expenses:			
Cost of revenues	679,402	384,038	251,266
Research and development	213,195	123,584	90,893
Sales, general and administrative	274,093	186,619	134,250
Write-off of in-process research and development	90,700	4,560	3,600
Amortization of acquisition related items including goodwill and other intangibles	17,915	–	–
Total operating costs and expenses	1,275,305	698,801	480,009
Operating income	384,053	322,192	181,974
Capital gain from merger of United Silicon Inc. with United Microelectronics Corp	–	674,728	–
Write-down of the United Microelectronics Corp Investment	(362,124)	–	–
Interest income and other	39,339	27,361	19,341
Interest expense	(165)	(9)	(11,916)
Income before provision for taxes on income, equity in joint venture and cumulative effect of change in accounting principle	61,103	1,024,272	189,399
Provision for taxes on income	25,845	378,006	54,925
Income before equity in joint venture and cumulative effect of change in accounting principle	35,258	646,266	134,474
Equity in income/(loss) of joint venture	–	6,184	(5,236)
Income before cumulative effect of change in accounting principle	35,258	652,450	129,238
Cumulative effect of change in accounting principle	–	–	(26,646)
Net income	**$ 35,258**	**$ 652,450**	**$ 102,592**
Net income per share:			
Basic			
Income before cumulative effect of change inaccounting principle	$ 0.11	$ 2.06	$ 0.44
Cumulative effect of change in accounting principle	–	–	(0.09)
Basic net income per share	$ 0.11	$ 2.06	$ 0.35
Diluted			
Income before cumulative effect of change in accounting principle	$ 0.10	$ 1.90	$ 0.42
Cumulative effect of change in accounting principle	–	–	(0.09)
Diluted net income per share	$ 0.10	$ 1.90	$ 0.33
Shares used in per share calculations:			
Basic	328,196	316,724	292,843
Diluted	353,345	343,479	308,620
Pro forma amounts with the change in accounting principle related to revenue recognition applied retroactively (unaudited):			
Net revenues	–	–	$ 661,983
Net income	–	–	$ 129,238
Net income per share:			
Basic	–	–	$ 0.44
Diluted	–	–	$ 0.42

See accompanying notes

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Consolidated Balance Sheets

(IN THOUSANDS EXCEPT PER SHARE AMOUNTS)	MARCH 31, 2001	2000
ASSETS		
Current assets:		
Cash and cash equivalents	$ 208,693	$ 85,548
Short-term investments	162,091	522,202
Accounts receivable, net of allowances for doubtful accounts, pricing adjustments and customer returns of $7,536 and $15,539 in 2001 and 2000, respectively	172,768	135,048
Inventories	342,453	131,307
Deferred income taxes	151,530	91,282
Advances for wafer purchases	–	22,485
Other current assets	64,344	53,053
Total current assets	1,101,879	1,040,925
Property, plant and equipment, at cost:		
Land	86,742	49,944
Building	218,234	98,674
Machinery and equipment	222,687	168,973
Furniture and fixtures	26,961	19,351
	554,624	336,942
Accumulated depreciation and amortization	(137,448)	(96,568)
Net property, plant and equipment	417,176	240,374
Long-term investments	288,972	185,073
Investment in United Microelectronics Corp	430,894	838,923
Developed technology and other assets	263,275	43,344
Total Assets	$ 2,502,196	$ 2,348,639
LIABILITIES AND STOCKHOLDERS' EQUITY		
Current liabilities:		
Accounts payable	$ 104,674	$ 56,361
Accrued payroll and related liabilities	28,776	29,796
Income tax payable	62,443	27,982
Deferred income on shipments to distributors	130,501	115,002
Interest payable and other accrued liabilities	24,016	15,571
Total current liabilities	350,410	244,712
Deferred tax liabilities	233,470	327,272
Commitments and contingencies		
Stockholders' equity:		
Preferred stock, $.01 par value; 2,000 shares authorized; none issued and outstanding	–	–
Common stock, $.01 par value; 2,000,000 shares authorized; 331,140 shares issued and outstanding at March 31, 2001; 325,512 shares issued and outstanding at March 31, 2000	3,311	3,255
Additional paid-in capital	725,626	487,634
Retained earnings	1,257,083	1,259,510
Treasury stock, at cost	(70,584)	–
Accumulated other comprehensive income	2,880	26,256
Total stockholders' equity	1,918,316	1,776,655
	$ 2,502,196	$ 2,348,639

See accompanying notes

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Consolidated Statements of Cash Flows

(IN THOUSANDS)	YEARS ENDED MARCH 31, 2001	2000	1999
Increase / (decrease) in Cash and Cash Equivalents			
Cash flows from operating activities:			
Net income	$ 35,258	$ 652,450	$ 102,592
Adjustments to reconcile net income to net cash provided by operating activities:			
Cumulative effect of change in accounting principle	–	–	26,646
Depreciation and amortization	93,451	44,191	32,112
Gain from available sales securities	(7,414)	–	–
Write-off of acquired in-process technology	90,700	4,560	3,600
Loss (gain) related to United Microelectronics Corp investment	362,124	(674,728)	–
Provision for deferred income taxes	–	254,444	(6,607)
Undistributed earnings of joint venture	–	(6,184)	5,236
Changes in assets and liabilities:			
Accounts receivable	(37,720)	(68,578)	(9,143)
Inventories	(186,708)	2,160	58,328
Prepaid assets	1,222	(31,201)	(4,556)
Deferred income taxes	(9,010)	22,537	(1,837)
Other assets	(54,056)	(15,242)	(957)
Accounts payable	44,244	33,035	(2,405)
Other accrued liabilities	3,592	13,054	33,509
Income taxes payable	(132,939)	(30,824)	(18,943)
Tax benefit from stock options	159,025	112,143	34,856
Deferred income on shipments to distributors	15,498	29,293	(8,806)
Total adjustments	342,009	(311,340)	141,033
Net cash provided by operating activities	377,267	341,110	243,625
Cash flows from investing activities:			
Purchases of available-for-sale investments	(2,389,366)	(2,506,365)	(1,177,948)
Proceeds from sale or maturity of available-for-sale investments	2,652,456	2,240,293	896,396
Purchases of held-to-maturity investments	–	–	(36,228)
Proceeds from maturity of held-to-maturity investments		34,358	36,145
Proceeds from sale of held-to-maturity investments	–	–	36,202
Investments in property, plant and equipment	(222,670)	(143,746)	(40,922)
Investment in joint venture	–	–	(5,448)
Assets purchased/obtained with acquisitions	4,243	(22,750)	(6,776)
Net cash provided by / (used in) investing activities	44,663	(398,210)	(298,579)
Cash flows from financing activities:			
Acquisition of treasury stock	(402,796)	(5,289)	(113,804)
Proceeds from issuance of common stock	81,802	84,315	55,481
Proceeds from sale of put warrants	22,209	10,038	–
Net cash provided by / (used in) financing activities	(298,785)	89,064	(58,323)
Net increase / (decrease) in cash and cash equivalents	123,145	31,964	(113,277)
Cash and cash equivalents at beginning of period	85,548	53,584	166,861
Cash and cash equivalents at end of period	$ 208,693	$ 85,548	$ 53,584
Schedule of non-cash transactions:			
Issuance of treasury stock under employee stock plans	$ 332,212	$ 10,400	$ 112,162
Issuance of treasury stock from debt conversion	–	–	53,503
Conversion of long term debt to common stock	–	–	250,322
Supplemental disclosures of cash flow information:			
Interest paid	165	9	12,992
Income taxes paid	$ 7,691	$ 11,881	$ 21,469

See accompanying notes

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Consolidated Statements of Stockholders' Equity

THREE YEARS ENDED MARCH 31, 2001 (IN THOUSANDS)	COMMON STOCK OUTSTANDING SHARES	COMMON STOCK OUTSTANDING AMOUNT	ADDITIONAL PAID-IN CAPITAL	RETAINED EARNINGS	TREASURY STOCK	ACCUMULATED OTHER COMPREHENSIVE INCOME	TOTAL STOCKHOLDERS' EQUITY
Balance at March 31, 1998	291,652	$ 2,916	$ 116,883	$ 504,468	$ (56,973)	$ (17,119)	$ 550,175
Components of comprehensive income:							
Net income	–	–	–	102,592	–	–	102,592
Unrealized gain on available-for-sale securities, net of tax expense of $87	–	–	–	–	–	130	130
Cumulative translation adjustment	–	–	–	–	–	(434)	(434)
Total comprehensive income							102,288
Issuance of common shares under employee stock plans	12,458	208	55,273	–	–	–	55,481
Issuance of common shares from convertible debt	19,608	–	250,322	–	–	–	250,322
Acquisition of treasury stock	(11,232)	–	–	–	(113,804)	–	(113,804)
Issuance of treasury stock under employee stock plans	–	–	(112,162)	–	112,162	–	–
Issuance of treasury stock from debt conversion	–	–	(53,503)	–	53,503	–	–
Tax benefit from exercise of stock options	–	–	34,856	–	–	–	34,856
Balance at March 31, 1999	312,486	3,124	291,669	607,060	(5,112)	(17,423)	879,318
Components of comprehensive income:							
Net income	–	–	–	652,450	–	–	652,450
Unrealized gain on available-for-sale securities, net of tax expense of $18,313	–	–	–	–	–	26,073	26,073
Cumulative translation adjustment	–	–	–	–	–	17,606	17,606
Total comprehensive income							696,129
Issuance of common shares under employee stock plans	13,272	131	84,184	–	–	–	84,315
Acquisition of treasury stock	(246)	–	–	–	(5,288)	–	(5,288)
Issuance of treasury stock under employee stock plans	–	–	(10,400)	–	10,400	–	–
Put option premiums	–	–	10,038	–	–	–	10,038
Tax benefit from exercise of stock options	–	–	112,143	–	–	–	112,143
Balance at March 31, 2000	325,512	3,255	487,634	1,259,510	–	26,256	1,776,655
Components of comprehensive income:							
Net income	–	–	–	35,258	–	–	35,258
Unrealized loss on available-for-sale securities, net of tax expense of $2,316	–	–	–	–	–	(22,831)	(22,831)
Cumulative translation adjustment	–	–	–	–	–	(545)	(545)
Total comprehensive income							11,882

Issuance of common shares under employee stock plans	9,382	93	82,737	–	–	–	82,830
Acquisition of treasury stock	(6,373)	(63)	–	–	(402,797)	–	(402,860)
Issuance of treasury stock under employee stock plans	–	–	(294,528)	(37,685)	332,213	–	
Issuance of shares for RocketChips	2,619	26	288,322	–	–	–	288,348
Put option premiums	–	–	22,209	–	–	–	22,209
Deferred Compensation – RocketChips	–	–	(19,773)	–	–	–	(19,773)
Tax benefit from exercise of stock options	–	–	159,025	–	–	–	159,025
Balance at March 31, 2001	331,140	$ 3,311	$ 725,626	$1,257,083	$ (70,584)	$ 2,880	$1,918,316

See accompanying notes

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Note 1. Nature of Operations

Xilinx designs, develops, and markets complete programmable logic solutions, including advanced integrated circuits, software design tools, predefined system functions delivered as cores of logic, design services, customer training, and field engineering support. The wafers used to manufacture our products are obtained from independent wafer manufacturers located in Taiwan and Japan. We are dependent upon these manufacturers to produce and deliver wafers on a timely basis. We are also dependent on subcontractors, located in the Asia Pacific region, to provide semiconductor assembly services. Xilinx is a global company with manufacturing and test facilities in the United States and Ireland and sales offices throughout the world. We derive approximately one-third of our revenues from international sales, primarily in Europe and Japan.

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Note 2. Summary of Significant Accounting Policies and Concentrations of Risk

Basis of presentation

The accompanying consolidated financial statements include the accounts of Xilinx and our wholly owned subsidiaries after elimination of all significant intercompany transactions. Our fiscal year ends on the Saturday nearest March 31. For ease of presentation, March 31 has been utilized as the fiscal year-end for all financial statement captions. Fiscal 2001 was a 52-week year ended on March 31, 2001. Fiscal 2000 was a 52-week year ended on April 1, 2000 and Fiscal 1999 was a 53-week year ended on April 3, 1999.

Certain amounts from the prior years have been reclassified to conform to the current year presentation.

Cash equivalents and investments

Cash and cash equivalents consist of cash on deposit with banks and investments in money market instruments and U.S. Treasury notes with minimal interest rate risk and original maturities of 90 days or less when acquired. Short-term investments consist of tax-advantaged municipal bonds, commercial papers, and tax-advantaged auction rate preferred municipal bonds with maturities greater than 90 days but less than one year from the balance sheet date. Restricted investments consisted of certificates of deposit held as collateral relating to leases for our facilities. Long-term investments consist of equity investments, U.S. Treasury notes, government agency bonds and tax-advantaged municipal bonds with maturities greater than one year, unless funds are specifically identified for current operations. We invest our cash, cash equivalents, short-term and long-term investments through various banks and investment banking and asset management institutions. This diversification of risk is consistent with our policy to maintain liquidity and ensure the collectibility of principal.

Management classifies investments as available-for-sale or held-to-maturity at the time of purchase and re-evaluates such designation at each balance sheet date, although classification is not generally changed. Securities are classified as held-to-maturity when we have the positive intent and the ability to hold the securities until maturity. Held-to-maturity securities are carried at cost adjusted for amortization of premiums and accretion of discounts to maturity. Such amortization, as well as any interest on the securities, is included in interest income. No investments were classified as held-to-maturity at March 31, 2001. Available-for-sale securities are carried at fair value with the unrealized gains or losses, net of tax, included as a component of accumulated other comprehensive income in stockholders' equity. Realized gains and losses and declines in value judged to be other-than-temporary on available-for-sale securities are included in other income. The fair values for marketable debt and equity securities are based on quoted market prices. The cost of securities matured or sold is based on the specific identification method.

Inventories

Inventories are stated at the lower of cost (first-in, first-out) or market (estimated net realizable value) and are comprised of the following at March 31, 2001 and 2000:

(IN THOUSANDS)	2001	2000
Raw materials	$ 26,245	$ 6,602
Work-in-progress	249,348	78,697
Finished goods	66,860	46,008
	$ 342,453	$ 131,307

Given the volatility of the market and the obsolescence in technology and shorter product life cycles, we write down inventories to net realizable value based on backlog and forecasted demand. However, backlog is subject to revisions, cancellations and rescheduling. Actual demand may differ from forecasted demand and such difference may have a material effect on our financial position and result of operations.

Advances for wafer purchases

In fiscal 1997, we signed an agreement with Seiko Epson, a primary wafer supplier. Repayment of this advance was received in the form of wafer deliveries, which began during the fourth quarter of fiscal 1998. The advance payment agreement also provided for interest to be paid to us in the form of free wafers. The repayment of this advance was completed during the second quarter of fiscal 2001.

Property, Plant and Equipment

Property, plant and equipment are stated at cost. Depreciation for financial reporting purposes is computed using the straight-line method over the estimated useful lives of the assets of three to five years for machinery, equipment, furniture and fixtures and up to thirty years for buildings. Depreciation expenses totaled $46.4 million, $33.3 million, and $27.5 million for fiscal year 2001, 2000, and 1999, respectively.

Revenue Recognition

We recognize revenue from product sales upon transfer of title to OEMs and end users. Reserves for sales returns and allowances are recorded at the time of shipment. As further explained in Note 3 of Notes to Consolidated Financial Statements, commencing in fiscal 1999, revenue on shipments to all distributors is deferred until products are sold by the distributors to end users. Prior to fiscal 1999, revenue on shipments to domestic distributors was deferred until resale to end users because arrangements with these distributors included returns and price protection privileges which could not be reasonably estimated. Revenue on all shipments to international distributors was recognized upon shipment to the distributor, with appropriate provision of reserves for returns and allowances.

Foreign currency translation

The U.S. dollar is the functional currency for our Ireland manufacturing facility. Assets and liabilities that are not denominated in the functional currency are remeasured into U.S. dollars, and the resulting gains or losses are included in "Interest income and other." The functional currency is the local currency for each of our other foreign subsidiaries. Assets and liabilities are translated at month-end exchange rates, and statements of operations are translated at the average exchange rates during the year. Exchange gains or losses arising from translation of foreign currency denominated assets and liabilities are included as a component of accumulated other comprehensive income in stockholders' equity.

Derivative financial instruments

As part of our ongoing asset and liability management activities, we periodically enter into financial arrangements to reduce financial market risks. These instruments are used to hedge foreign currency, equity and interest rate market exposures of underlying assets and liabilities. We do not enter into derivative financial instruments for trading purposes.

Our accounting policies for these instruments are based on whether such instruments are designated as hedging transactions. The criteria we use for designating an instrument as a hedge includes the instrument's effectiveness in risk reduction and one-to-one matching of derivative instruments to underlying transactions. Gains and losses on foreign currency forward and option contracts that are designated and effective as hedges of anticipated transactions, for which a firm commitment has been attained, are deferred and either recognized in income or included in the basis of the transaction in the same period that the underlying transactions are settled. Gains and losses on foreign currency forward and option contracts and interest rate swap contracts that are designated and effective as hedges of existing transactions are recognized in income in the same period as losses and gains on the underlying transactions are recognized and generally offset. Gains and losses on any instruments not meeting the above criteria are recognized in income in the current period. If an underlying hedged transaction is terminated earlier than initially anticipated, the offsetting gain or loss on the related derivative instrument is recognized in income in the same period. Subsequent gains or losses on the related derivative instrument are recognized in income in each period until the instrument matures, is terminated or is sold. Premiums paid for foreign currency forward and option contracts are generally amortized over the life of the contracts and are not material to our results of operations. Unamortized premiums are included in prepaid expenses and other current assets.

Employee stock plans

We account for our stock option and employee stock purchase plans in accordance with provisions of the Accounting Principles Board's Opinion No. 25 (APB 25), "Accounting for Stock Issued to Employees." In addition, we disclose pro forma information related to our stock plans according to Financial Accounting Standards Board's Statement No. 123, "Accounting for Stock-Based Compensation" (FASB 123).

Use of estimates

The preparation of financial statements in conformity with accounting principles generally accepted in United States requires management to make estimates and assumptions that affect the reported amounts of assets and liabilities and disclosure of contingent liabilities at the date of the financial statements and the reported amounts of net revenues and expenses during the reporting period. Such estimates relate to the useful lives of fixed assets and intangible assets, inventory write-downs, allowances for doubtful accounts, pricing adjustments, customer returns, potential reserves relating to litigation matters as well as other accruals or reserves. Actual results may differ from those estimates, and such differences may be material to the financial statements.

New Accounting Pronouncements

In June 1998, the Financial Accounting Standards Board issued Statement of Financial Accounting Standards No. 133, (FASB 133), "Accounting for Derivative Instruments and Hedging Activities," which requires adoption by Xilinx beginning April 2001. The effect of adopting the Standard will not be material to our consolidated results of operations or financial position. FASB 133 will require us to recognize all derivatives on the balance sheet at fair value. Derivatives that are not hedges must be adjusted to fair value through income. If the derivative is a hedge, depending on the nature of the hedge, changes in the fair value of the derivative will either be offset against the change in fair value of the hedged assets, liabilities, or firm commitments through earnings or recognized in accumulated other comprehensive income until the hedged item is recognized in earnings. The ineffective portion, if any, of a derivative's change in fair value will be immediately recognized in earnings.

In December 1999, the Securities and Exchange Commission (SEC) issued SEC Staff Accounting Bulletin No. 101 (SAB 101), "Revenue Recognition in Financial Statements." SAB 101 summarizes certain of the SEC's views in applying generally accepted accounting principles to revenue recognition in financial statements. We adopted SAB 101 in the fourth quarter of fiscal 2001 and the adoption did not have a material effect on our consolidated results of operations or financial position.

In March 2000, the FASB issued FASB Interpretation No.44 ("FIN 44"), "Accounting for Certain Transactions Involving Stock Compensation — an Interpretation of APB Opinion No. 25." FIN 44 is intended to clarify the application of APB Opinion No. 25 by providing guidance regarding among other issues: the definition of an employee for purposes of applying APB Opinion No. 25; the criteria for determining whether a plan qualifies as a noncompensatory plan; the accounting consequence of various modifications to the terms of the previously fixed stock options or awards; and the accounting for an exchange of stock compensation awards in a business combination. FIN 44 was effective July 1, 2000 but certain provisions covered specific events occurring after December 15, 1998 or January 12, 2000. The adoption of FIN 44 did not have a material impact on our consolidated financial position or results of operations.

In November 2000, the FASB's Emerging Issues Task Force ("EITF") reached final consensuses on EITF Issue No. 00-19, "Determination of Whether Share Settlement is Within the Control of the Issuer" for purposes of applying EITF Issue No. 96-13, "Accounting for Derivative Financial Instruments Indexed to, and Potentially Settled in, a Company's Own Stock." EITF 00-19 addresses and clarifies whether specific contract provisions or other circumstances cause a net-share or physical settlement alternative to be within or outside the control of the issuer. EITF 96-13 addresses accounting for equity derivative contracts indexed to, and potentially settled in, a company's own stock by providing guidance for distinguishing between permanent equity, temporary

equity and assets and liabilities. Under EITF 00-19, equity derivatives that were issued prior to September 20, 2000, and classified as permanent equity must meet certain criteria or be re-classified as temporary equity. To qualify as permanent equity all the following criteria must be met: the equity derivative contract must permit the company to settle in unregistered shares, the company must have sufficient authorized but unissued shares available to settle the contract, the contract must contain an explicit limit on the number of shares to be delivered in a share settlement, there can be no requirement in the contract to post collateral, there can be no "make whole" provisions in the contract requiring cash settlement and there can be no provisions in the contract that indicate the counterparty has rights that rank higher than those of a common shareholder. Compliance with EITF 00-19 did not have a material impact on the Company's consolidated financial position.

Concentrations of credit risk

We attempt to mitigate the concentration of credit risk in our trade receivables with respect to the high-technology industry with our credit evaluation process, relatively short collection terms, distributor agreements, sales among various end-user applications throughout the high-technology market and the geographical dispersion of sales. We generally do not require collateral. Bad debt write-offs have been insignificant for all years presented.

No end customer accounted for more than 10% of revenues in 2001, 2000, or 1999. Approximately 27%, 27% and 20% of net revenues were recognized through our largest domestic distributor in 2001, 2000, and 1999, respectively. A second domestic distributor accounted for approximately 24%, 24%, and 17% of net revenues in fiscal 2001, 2000 and 1999, respectively.

On a consolidated basis, at March 31, 2001, two distributors accounted for 59.3% and 28.0% of total accounts receivable. These two distributors also accounted for 44.1% and 28.6% of worldwide net revenues in fiscal 2001. (See ITEM 1. Business: Marketing and Sales; Backlog and Customers)

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Note 3. Accounting Change – Deferred Revenue Recognition on Sales to International Distributors

During the fourth quarter of fiscal 1999, we changed our accounting method for recognizing revenue on all shipments to international distributors. The change was made retroactive to the beginning of fiscal 1999. While we previously deferred revenue on shipments to domestic distributors until the products were sold to the end user, we recognized revenue upon shipment to international distributors, net of appropriate reserves for returns and allowances. Following the accounting change, revenue recognition on shipments to distributors worldwide is deferred until the products are sold to the end customer. We believe that deferral of revenue on shipments to distributors until the product is shipped by the distributor to an end customer is a more meaningful measurement of results of operations, and is consistent with industry practice. The cumulative effect of the change in accounting method for fiscal 1999 was a charge of $26.6 million, net of $12.0 million in taxes, or $0.09 net income per diluted share.

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Note 4. Joint Venture

Xilinx, UMC and other parties entered into a joint venture to construct a wafer fabrication facility in Taiwan, known as USIC. We had a 20% equity ownership in USIC and had the right to receive up to 31.25% of the wafer capacity from this facility. We accounted for this investment using the equity method of accounting with a one-month lag in recording our share of results for the entity. In fiscal 2000 net gains were generated as USIC entered volume wafer production and shipment, while the fiscal 1999 net loss was a result of the continued ramp up in production of the wafer fabrication facility.

In January 2000 USIC was merged into UMC and our equity position in USIC was converted into shares of UMC which are publicly traded on the Taiwan Stock Exchange. We recognized a non-cash gain of $674.7 million ($398.1 million net of taxes) in our fiscal 2000 fourth quarter as a result of the merger of USIC into UMC. The gain represents the appreciation of our investment in USIC. As a result of this merger, we owned approximately 222 million shares of UMC common stock, which represent approximately 2% of the combined UMC Group. In July 2000, we received a 20% stock dividend, which increased our investment holdings in UMC to approximately 266 million shares. We retain equivalent wafer capacity rights in UMC as we previously had in USIC, as long as we retain a percentage of our shares of UMC common stock. If our holdings fall below the specified level, our wafer capacity rights would be decreased prorated by the UMC shares we hold.

Due to restrictions imposed by UMC and the Taiwan Stock Exchange, the majority of our UMC shares could not be sold until July 2000. These regulatory restrictions will gradually expire between July 2000 and January 2004. At March 31, 2001, the restricted portion of our UMC investment totaled $179.5 million.

The Company accounts for the portion (approximately 58% at March 31, 2001) of its investment in UMC which becomes unrestricted within twelve months as available-for-sale marketable security in accordance with SFAS 115. The portion of the investment in UMC which is restricted beyond twelve months (approximately 42% of the Company's holdings at March 31, 2001) is accounted for as a cost method investment classified as a long-term investment.

Due to the current weakness in the semiconductor industry, the value of our UMC shares declined to $430.9 million as of March 31, 2001. The downturn in the semiconductor industry, and the economy in general, appears to be more severe than previously anticipated, and there is a great deal of uncertainty regarding when the semiconductor industry will recover from this down cycle. Because of the continued downturn in the economy, we believed that the decline in the market value of our investment in UMC as of March 31, 2001, was other than temporary as defined by accounting principles generally accepted in the United States. In the fourth quarter of fiscal 2001 we recognized a pre-tax loss of $362.1 million. If the value our UMC shares declines further, we may be required to record additional losses. In addition, in future periods, we may recognized a gain or loss if we sell our UMC shares due to fluctuations in the market value of UMC stock.

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Note 5. Financial Instruments

Cash and Investments

The following is a summary of available-for-sale securities:

(IN THOUSANDS)	MARCH 31, 2001 AMORTIZED COST	GROSS UNREALIZED GAINS	GROSS UNREALIZED LOSSES	ESTIMATED FAIR VALUE	MARCH 31, 2000 AMORTIZED COST	GROSS UNREALIZED GAINS	GROSS UNREALIZED LOSSES	ESTIMATED FAIR VALUE
Money market funds	$ 160,093	$ –	$ –	$ 160,093	$ 93,172	$ –	$ –	$ 93,172
Commercial paper	127,142	–	–	127,142	62,712	–	–	62,712
U.S. Treasury notes	–	–	–	–	5,005	–	–	5,005
Auction rate preferred	21,512	3	–	21,515	335,039	1	(14)	335,026
Government agency bonds	–	–	–	–	9,925	–	(142)	9,783
Municipal bonds	339,691	5,610	(32)	345,269	300,897	370	(1,513)	299,754
Investment in UMC	251,355	–	–	251,355	396,509	45,904	–	442,413
	$ 899,793	$ 5,613	$ (32)	$ 905,374	$1,203,259	$ 46,275	$ (1,669)	$1,247,865
Included in:								
Cash and cash equivalents				$ 202,956				$ 98,177
Short-term investments				162,091				522,202
Long-term investments				288,972				185,073
Investment in UMC				251,355				442,413
				$ 905,374				$1,247,865

For fiscal 2001, interest and other income included a pre-tax gain on our investment in Nuron LLC of $4.5 million. The gain was recorded under guidance from Emerging Issues Task Force Bulletin 91-5 "Non-Monetary Exchange of Cost-Method investments."

Derivatives

In fiscal 2001, we utilized forward currency contracts to protect against the net yen exposure created when we began purchasing most of our wafers from Japanese suppliers in U.S. dollars yet continued to invoice Japanese customers in yen. Realized gain of $ 0.9 million in fiscal 2001 and loss of $0.5 million in fiscal 2000 were offset against revenue when there was a firm commitment, otherwise they were included in "Interest income and other." At March 31, 2000, no commitments under foreign currency forward or option contracts were outstanding.

At March 31, 2001, we have four outstanding forward currency exchange contracts against Irish Pounds with Bank of America. Total value of contracts is $10 million U.S. dollars. The four contracts expire at various dates: May 15, June 15, August 15, and September 14 in year 2001.

Lines of Credit

We had $40 million available under a syndicated bank revolving credit line agreement, which expired in March 2001 and we decided not to extend this line of credit. Additionally, our Ireland manufacturing facility has an additional $6.2 million available under a multicurrency credit line, which expires in November 2001. Under this agreement, borrowings bear interest at the bank's prime rate or 0.75% over the Euribor rate. At March 31, 2000, no borrowings were outstanding under any credit lines. We are in full compliance with the agreement's required covenants and financial ratios. The agreements prohibit the payment of cash dividends without prior bank approval.

Subordinated Notes

In fiscal 1999, we converted in full $250.0 million of 5 1/4% Convertible Subordinated Notes due 2002 for a total of 19.6 million shares of common stock at a price of $12.75 per share.

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Note 6. Commitments

We lease some of our manufacturing and office facilities under operating leases that expire at various dates through December 2014. Lease agreements for certain corporate facilities contain payment provisions, which allow for changes in rental amounts based upon interest rate changes. The approximate future minimum lease payments under operating leases are as follows:

YEARS ENDED MARCH 31,	(IN THOUSANDS)
2002	$ 3,389
2003	2,747
2004	1,277
2005	926
2006	485
Thereafter	3,547
	$ 12,371

Rent expense was approximately $2.5 million for fiscal 2001, $7.3 million for fiscal year 2000, and $4.5 million for 1999. The decreased rent expense in fiscal 2001 was due to the acquisition of buildings in San Jose, California during fiscal year 2001.

During fiscal 1998, we entered into an agreement for a facility to be built on property adjacent to our corporate facilities, which was completed in fiscal 2000. Upon signing the lease agreement, we paid the lessor $31.3 million for prepaid rent and an option to purchase the facility. The rent prepayment covered one year and was discounted to its present value. We exercised the lease agreement's purchase option in fiscal 2000 and the prepaid purchase option was considered payment in full.

In December 1999, we exercised another option to purchase three buildings previously leased at our San Jose corporate facility. The restricted investment of $34.4 million related to certain collateral requirements on the building leases and was later used to purchase the three buildings.

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Note 7. Net Income Per Share

Basic net income per share is computed by dividing net income by the weighted average number of common shares outstanding during the period. In computing diluted net income per share, the average stock price for the period is used in determining the number of shares assumed to be purchased from the exercise of stock options. Diluted earnings per share is computed using the weighted average common and dilutive common equivalent shares outstanding.

The computation of basic net income per share for all years presented is derived from the information on the face of the income statement, and there are no reconciling items in either the numerator or denominator. Additionally, there are no reconciling items in the numerator used to compute diluted net income per share. The total shares used in the denominator of the diluted net income per share calculation includes 25.1 million, 26.8 million and 15.8 million incremental common shares attributable to outstanding options for fiscal years 2001, 2000, and 1999, respectively.

Before the long-term debt was converted to equity in the amount of approximately 19.6 million shares in February 1999, they were not included in the calculation of diluted net income per share, as their inclusion would have had an anti-dilutive effect for all periods presented. Outstanding options to purchase approximately 4.3 million, 0.3 million, and 9.6 million shares, for the fiscal years 2001, 2000 and 1999, respectively, under the Company's Stock Option Plans were not included in the treasury stock calculation to derive diluted net income per share as their inclusion would have had an anti-dilutive effect. In addition, the put warrants disclosed in Note 9 did not have any impact on basic or diluted net income per share in fiscal March 31, 2001 as their inclusion would have had an anti-dilutive effect.

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Note 8. Comprehensive Income

FASB 130 established standards for the reporting and disclosure of comprehensive income and its components; however, the disclosure has no impact on our consolidated results of operations, financial position or cash flows. Comprehensive income is defined as the change in equity of a company during a period resulting from certain transactions and other events and circumstances, excluding transactions resulting from investments by owners and distributions to owners. The difference between net income and comprehensive income for Xilinx is from foreign currency translation adjustments and unrealized gains or losses on our available-for-sale securities.

The components of comprehensive income are as follows:

(IN THOUSANDS)	MARCH 31, 2001	2000	1999
Net income	$ 35,258	$ 652,450	$ 102,592
Cumulative translation adjustment	(545)	17,606	(434)
Unrealized gain (loss) on available for sale securities, net of tax	(22,831)	26,073	130
Comprehensive income	$ 11,882	$ 696,129	$ 102,288

The components of accumulated other comprehensive income (loss) are as follows:

(IN THOUSANDS)	MARCH 31, 2001	2001	1999
Cumulative translation adjustment	$ (594)	$ (49)	$ (17,655)
Unrealized gain on available for sale securities, net of tax	3,474	26,305	232
Accumulated other comprehensive income (loss)	$ 2,880	$ 26,256	$ (17,423)

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Note 9. Stockholders' Equity

The Company's Certificate of Incorporation authorized 2 million shares of undesignated preferred stock. The preferred stock may be issued in one or more series. The Board of Directors is authorized to determine or alter the rights, preferences, privileges and restrictions granted to or imposed upon any wholly unissued series of preferred stock. As of March 31, 2001 and 2000 no preferred shares were issued or outstanding.

Treasury stock and put options

We authorized a stock buyback program in September 1998 and June 2000 whereby up to $100 million and $200 million dollars, respectively, of our common stock could be purchased in the open market from time to time as market and business conditions warranted. This program was completed in November 2000. In November 2000, additional stock repurchase programs were authorized to buyback up to $250 million dollars of our common stock. We have reissued treasury shares repurchased in response to Employee Stock Option exercises and Employee Qualified Stock Purchase Plan requirements as well as in conjunction with our redemption of convertible debt. During fiscal 2001 and 2000, we repurchased a total of 6.4 million and 0.2 million shares of common stock for $402.8 million and $5.3 million, respectively. In fiscal 2001 and 2000, 5.0 million and 0.5 million shares were reissued, respectively. As of March 31, 2001, we held 1.4 million shares of treasury stock in conjunction with the stock repurchase program. During fiscal 2001, we sold put warrants that entitle the holder of each warrant to sell to us, by physical delivery, one share of common stock at a specified price, ranging from $52 to $72 per share. The outstanding put warrants will expire at various dates through February 2002. As of March 31, 2001, we have 1.4 million shares subject to future issuance under of outstanding put warrants.

Stockholder Rights Plan

In October 1991, we adopted a stockholder rights plan and declared a dividend distribution of one preferred stock purchase right for each outstanding share of common stock. The rights become exercisable based upon the occurrence of certain conditions including acquisitions of Company stock, tender or exchange offers and certain business combination transactions of the Company. In the event one of the conditions is triggered, each right entitles the registered holder to purchase a number of shares of preferred stock of the Company or, under limited circumstances, of the acquirer. The rights are redeemable at the Company's option, under certain conditions, for $.01 per right and expire on October 4, 2001.

Employee Stock Option Plans

Under existing stock option plans (Option Plans), options reserved for future issuance to employees and directors of the Company total 54.4 million shares as of March 31, 2001. Options to purchase shares of our common stock under the Option Plans are granted at 100% of the fair market value of the stock on the date of grant. Options granted to date expire ten years from date of grant and vest at varying rates over four or five years.

A summary of our Option Plans activity, and related information are as follows:

YEARS ENDED MARCH 31,	2001		2000		1999	
	SHARES (000)	WEIGHTED AVERAGE EXERCISE PRICE	SHARES (000)	WEIGHTED AVERAGE EXERCISE PRICE	SHARES (000)	WEIGHTED AVERAGE EXERCISE PRICE
Outstanding at beginning of year	55,333	$ 12.19	63,158	$ 9.50	58,098	$ 6.67
Granted	7,813	63.51	4,149	37.24	18,560	15.04
Exercised	(8,008)	7.41	(10,997)	6.03	(10,844)	3.98
Forfeited	(714)	33.26	(977)	13.74	(2,656)	9.03
Outstanding at end of year	54,425	$ 19.98	55,333	$ 12.19	63,158	$ 9.50
Shares available for grant	35,569		28,564		5,624	

The following information relates to options outstanding and exercisable under the Option Plan at March 31, 2001:

	OPTIONS OUTSTANDING			OPTIONS EXERCISABLE	
RANGE OF EXERCISE PRICES	OPTIONS OUTSTANDING (000)	WEIGHTED AVERAGE REMAINING CONTRACTUAL LIFE (YEARS)	WEIGHTED AVERAGE EXERCISE PRICE	OPTIONS EXERCISABLE (000)	WEIGHTED AVERAGE EXERCISE PRICE

$ 0.57 – $ 8.25	16,000	3.95	$ 5.78	15,754	$ 5.76
$ 8.31 – $ 11.72	14,460	6.50	9.89	11,012	9.92
$ 11.97 – $ 34.03	14,523	7.32	18.51	9,085	16.77
$ 34.44 – $ 96.63	9,442	9.11	61.78	1,691	56.62
$ 0.57 – $ 96.63	54,425	6.42	$ 19.98	37,542	$ 11.94

At March 31, 2000, 33.6 million options were exercisable at an average price of $8.37.

Employee Qualified Stock Purchase Plan

Under our 1990 Employee Qualified Stock Purchase Plan (Stock Purchase Plan), qualified employees can elect to have up to 15 percent of their annual earnings withheld, up to a maximum of $21,250, to purchase our common stock at the end of six-month enrollment periods. The purchase price of the stock is 85% of the lower of the fair market value at the beginning of the twenty-four month offering period or at the end of each six-month purchase period. Almost all employees are eligible to participate. Under this plan, 1.4 million and 2.3 million shares were issued during 2001 and 2000, respectively, and 8.0 million shares were available for issuance at March 31, 2001.

Stock-Based Compensation

As permitted under FASB Statement No. 123, "Accounting for Stock-Based Compensation" (FASB 123), we have elected to continue to follow Accounting Principles Board Opinion No. 25, "Accounting for Stock Issued to Employees" (APB 25) and related Interpretations in accounting for our stock-based awards to employees. Under APB 25, the Company generally recognizes no compensation expense with respect to such awards.

Pro forma information regarding net income and earnings per share is required by FASB 123 and has been determined as if we had accounted for awards to employees under the fair value method of FASB 123. The fair value of stock options and stock purchase plan rights under the Option Plans and Stock Purchase Plan was estimated as of the grant date using the Black-Scholes option pricing model. The Black-Scholes model was originally developed for use in estimating the fair value of traded options and requires the input of highly subjective assumptions including expected stock price volatility. Our stock options and stock purchase plan rights have characteristics significantly different from those of traded options, and changes in the subjective input assumptions can materially affect the fair value estimate. The fair value of stock options and stock purchase plan rights granted in fiscal years 2001, 2000 and 1999 were estimated at the date of grant assuming no expected dividends and the following weighted average assumptions.

YEARS ENDED MARCH 31,	STOCK OPTIONS			STOCK PURCHASE PLAN RIGHTS		
	2001	2000	1999	2001	2000	1999
Expected life (years)	3.50	3.50	3.00	0.50	0.50	0.50
Expected stock price volatility	0.71	0.65	0.65	0.79	0.67	0.64
Risk-free interest rate	5.9%	5.8%	5.0%	5.6%	5.3%	5.0%

For purposes of pro forma disclosures, the estimated fair value of stock-based awards is amortized against pro forma net income over the stock-based awards' vesting period. Had we accounted for stock-based awards to employees under FASB 123, our net income (loss) would have been $(100.2) million, $560.3 million, and $65.2 million in 2001, 2000, and 1999, respectively. Basic net income(loss) per share would have been $(0.31), $1.73, and $0.22 in 2001, 2000, and 1999, respectively, while diluted net income(loss) per share would have been $(0.31), $1.60, and $0.21, respectively.

Calculated under FASB 123, the weighted-average fair value of the stock options granted during 2001, 2000, and 1999 was $37.91, $18.87, and $6.90 per share, respectively. The weighted-average fair value of stock purchase rights granted under the Stock Purchase Plan during 2001, 2000, and 1999 were $27.31, $18.19, and $4.98 per share, respectively.

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Note 10. Income Taxes

(IN THOUSANDS)		YEARS ENDED MARCH 31, 2001	2000	1999
Federal:	Current	$ 131,903	$ 97,019	$ 45,482
	Deferred	(124,263)	196,172	(3,558)
		7,640	293,191	41,924
State:	Current	21,678	15,851	9,187
	Deferred	(30,087)	58,272	(3,049)
		(8,409)	74,123	6,138
Foreign:	Current	26,614	10,692	6,863
Total		$ 25,845	$ 378,006	$ 54,925

The tax benefits associated with stock options exercises and the employee stock purchase plan resulted in a tax benefit of $159.0 million, $112.1 million, and $34.9 million, for fiscal years 2001, 2000, and 1999, respectively. Such benefits are credited to additional paid-in capital when realized. The Company has tax loss and credit carryforwards of approximately $36 million and $31 million respectively, if unused these carryforwards will expire in 2005 through 2021. Pretax income from foreign operations was $281.5 million, $106.4 million, and $61.2 million for fiscal years 2001, 2000, and 1999, respectively. Unremitted foreign earnings that are considered to be permanently invested outside the United States and on which no deferred taxes have been provided, accumulated to approximately $193 million as of March 31, 2001. The residual U.S. tax liability, if such amounts were remitted, would be approximately $48.2 million.

The provision for income taxes reconciles to the amount obtained by applying the Federal statutory income tax rate to income before provision for taxes as follows:

(IN THOUSANDS)	YEARS ENDED MARCH 31, 2001	2000	1999
Income before provision for taxes	$ 61,103	$ 1,024,272	$ 189,399
Federal statutory tax rate	35%	35%	35%
Computed expected tax	$ 21,386	$ 358,495	$ 66,290
State taxes net of federal benefit	(5,468)	48,180	3,990
Tax exempt interest	(6,734)	(5,472)	(3,822)
Foreign earnings at lower tax rates	(9,488)	(15,370)	(4,415)
In-Process R&D Charge	31,745	-	-
Amortization of Goodwill	4,143	-	-
Tax Credits	(10,640)	(6,095)	(5,574)
Other	901	(1,732)	(1,544)
Provision for taxes on income	$ 25,845	$ 378,006	$ 54,925

The major components of deferred tax assets and liabilities consist of the following:

(IN THOUSANDS)	YEARS ENDED MARCH 31, 2001	2000
Deferred tax assets:		
Inventory valuation differences	$ 26,227	$ 10,725
Deferred income on shipments to distributors	83,701	76,262
Nondeductible accrued expenses	9,711	5,948
Tax carryforwards	29,445	-

Other	3,971	(1,453)
Total	153,055	91,482
Deferred tax liabilities:		
Intangible and Fixed Assets	(11,874)	4,023
Unremitted foreign earnings	(83,932)	(36,453)
Capital gain from merger of USIC with UMC	(133,599)	(276,638)
Current net value of investments	(2,674)	(18,313)
Other	(1,391)	617
Total net deferred tax liability	(233,470)	(326,764)
Total net deferred tax (liabilities) assets	$ (80,415)	$ (235,282)

On December 28, 2000, the Internal Revenue Service issued a statutory notice of deficiency reflecting proposed audit adjustments for the fiscal years 1996, 1997, and 1998. We filed a petition with the Tax Court on March 26, 2001 contesting this notice of deficiency. We believe we have meritorious defenses to the proposed adjustments and sufficient taxes have been provided.

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Note 11. Segment Information

We operate and track our results in one operating segment. We design, develop, and market programmable logic semiconductor devices and the related software design tools.

Enterprise wide information is provided in accordance with FASB 131. Geographic revenue information for the fiscal years 2001, 2000, and 1999 is based on the shipment location. Long-lived assets include property, plant and equipment as well as intangible assets including developed technology, assembled workforce, and goodwill. Property, plant and equipment information is based on the physical location of the asset at the end of each fiscal year while the intangible assets are based on the location of the owning entity.

Net revenues from unaffiliated customers by geographic region were as follows:

(IN THOUSANDS)	YEARS ENDED MARCH 31, 2001	2000	1999
North America	$ 1,028,185	$ 681,078	$ 447,147
Europe	334,002	201,772	139,815
Japan	163,567	82,581	47,522
Asia Pacific	133,604	55,562	27,499
	$ 1,659,358	$ 1,020,993	$ 661,983

Net long-lived assets by country were as follows:

(IN THOUSANDS)	YEARS ENDED MARCH 31, 2001	2000
North America	$ 538,983	$ 207,769
Ireland	63,172	35,370
Other	22,346	26,375
	$ 624,501	$ 269,514

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Note 12. Litigation

On June 7, 1993, we filed suit against Altera Corporation (Altera) in the United States District Court for the Northern District of California for infringement of certain of our patents. Subsequently, Altera filed suit against Xilinx, alleging that certain of our products infringe certain Altera patents. As a result of certain motions and rulings in the case, Altera is left with one claim against Xilinx, which remains the subject of a Company motion for summary judgment. A ruling on this motion is pending. If the remaining claim against Xilinx survives the motion for summary judgment, it will be decided at a trial, which is unscheduled at this point. The Court's rulings also dismissed certain claims by us, leaving intact claims of infringement by Altera under two Company patents. The remaining claims against Altera were decided at a trial which began on October 18, 2000. On November 17, 2000, a federal jury found that the two Company patents in the case were valid and that Altera infringed both patents. On May 10, 2001, the trial judge overturned the jury verdict, by granting Altera’s motion to enter Judgment as a Matter of Law. The judge found that the Altera Flex 8000 product does not infringe one of the two Company patents, and that the other Company patent is invalid. The Company has filed its notice of appeal to reinstate the jury verdict, although no timetable for appeal has been set.

On April 20, 1995, Altera filed an additional suit against Xilinx in the Federal District Court in Delaware, alleging that our XC5200 family infringes an Altera patent. We answered the Delaware suit denying that the XC5200 family infringes the patent in suit, asserting certain affirmative defenses and counterclaiming that the Altera Max 9000 family infringes certain of our patents. The Delaware suit was transferred to the United States District Court for the Northern District of California.

On July 22, 1998, Altera and Joseph Ward, a former Xilinx employee, filed suit against Xilinx in Superior Court in Santa Clara County, California, arising out of our efforts to prevent disclosure of certain Company confidential information. Altera's suit requests declaratory relief and claims Xilinx engages in unfair business practices and interference with contractual relations. On September 10, 1998 we filed cross claims against Altera and Ward for unfair competition and breach of contract, among other claims, in the California action. On October 20, 1998, Altera and Ward filed crossclaims against Xilinx for malicious prosecution of civil action and defamation. On September 15, 1999, the Court dismissed all of our claims against Altera and Mr. Ward, finding that we were unable to show any damages we suffered as a result of any actions by Mr. Ward. On May 24, 2001, the Court dismissed all of Altera’s claims against the Company leaving only Mr. Ward’s claims of defamation against the Company.

On May 31, 2000, Altera filed an additional suit against Xilinx in the Federal District Court for the Northern District of California, alleging that certain Xilinx products, including our Virtex FPGAs, infringe three Altera patents. Altera's suit requests unspecified monetary damages as well as issuance of an injunction to prevent Xilinx from selling allegedly infringing parts. Xilinx has filed an amended answer and countercomplaint denying the allegations and alleging that the Altera patents are invalid and unenforceable because Altera engaged in inequitable conduct in acquiring the asserted patents. The counterclaim also alleges that Altera is infringing three additional Company patents. A claims construction hearing to determine the interpretation of Altera's patent claims was held on April 26 and 27, 2001. No decision has been rendered by the judge.

On November 16, 2000, we requested that the International Trade Commission investigate alleged infringements by Altera of three Company patents, and if so, to bar Altera from importing or selling such products into the United States. On December 18, 2000, the International Trade Commission decided to investigate our claims against Altera. A hearing has been set for June 25, 2001.

On March 9, 2001, the ITC at the request of Altera initiated an investigation against Xilinx based on two additional Altera patents. The matter has been assigned to Judge Harris, the same administrative law judge handling the ITC action by Xilinx against Altera. A hearing has been set for September 24, 2001.

The ultimate outcome of these matters cannot be determined at this time. Management believes that it has meritorious defenses to such claims and is defending them vigorously. The foregoing is a forward-looking statement subject to risks and uncertainties, and the future outcome of these matters could differ materially due to the uncertain nature of each legal proceeding and because most of the lawsuits are still in the pre-trial stages.

There are no other pending legal proceedings of a material nature to which we are a party or of which any of our property is the subject. Other than the petition filed by the Company with the Tax Court on March 26, 2001, we know of no legal proceedings contemplated by any governmental authority or agency.

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Note 13. Business Combination

On November 9, 2000, we completed the acquisition of RocketChips, Inc., a privately held fabless semiconductor company. RocketChips is a developer of ultra-high-speed CMOS mixed-signal transceivers serving the networking, wireless and wired telecommunications, and enterprise storage markets.

In connection with the acquisition, we issued approximately 2,806,000 shares of Common stock in exchange for all outstanding preferred and common stock of RocketChips and reserved approximately 807,000 additional shares of Common stock for issuance upon exercise of outstanding employee stock options of RocketChips. Of the shares issued, approximately 380,000 shares of Xilinx's Common stock are being held in escrow for a period of one year following the acquisition for the purpose of providing a fund against which Xilinx may seek indemnification from former RocketChips stockholders for any breaches of representations, warranties or covenants under the Merger Agreement.

The acquisition was accounted for under the purchase method of accounting. The purchase price of RocketChips was allocated to the fair value of the specific tangible and intangible assets acquired and liabilities assumed from RocketChips pursuant to an independent valuation. The total purchase price for RocketChips was $291.2 million, consisting of $231.0 million of Xilinx Common stock, $57.3 million of options to purchase Xilinx common stock and $2.8 million of acquisition related costs. Xilinx recorded a charge to operations upon consummation of the transaction for acquired in-process research and development of approximately $90.7 million. In addition, Xilinx recorded approximately $218.9 million of intangible assets, goodwill, and deferred compensation on the balance sheet, which resulted in amortization expense of approximately $22.4 million in fiscal 2001.

The projects identified as in-process will require additional effort in order to establish technological feasibility. These projects have identifiable technological risk factors that indicate that even though successful completion is expected, it is not assured. If an identified project is not successfully completed there is no alternative future use for the project and the expected future income will not be realized. To determine the value of the in-process research and development, the expected future cash flow attributable to the in-process technology was discounted, taking into account the percentage of completion, utilization of preexisting of "core" technology, risks related to the characteristics and applications of the technology, existing and future markets, and technological risk associated with completing the development of the technology. The valuation approach used was a form of discounted cash flow approach known as the "percentage of completion" approach. We immediately expensed this in-process research and development upon consummation of the acquisition in the third quarter of fiscal 2001.

Deferred compensation recorded in connection with the acquisition represents the estimated intrinsic value of unvested RocketChips stock options assumed by Xilinx in the merger agreement for which employee service is required after the closing date of the merger in order for the options to vest. Deferred compensation will be amortized to expense over the remaining vesting period of the options.

Below is a table of the acquisition cost and amortization period of the intangible assets.

	AMOUNT (IN MILLIONS)	AMORTIZATION LIFE
Deferred compensation	$ 24.3	1 month-4 years
Goodwill	140.5	5 years
Developed technology	6.6	5 years
Noncompete agreement	23.6	3 years
Patents	13.2	7 years
Other intangibles	10.7	2-3 years
Total	$ 218.9	

We completed the acquisition of Philips Semiconductors' line of low—power complex programmable logic devices (CPLDs) on August 2, 1999. The total cost, including acquisition related fees, was approximately $22.8 million. The purchase price allocation, based on an independent appraisal, resulted in a $4.6 million charge to research and development in the second quarter of fiscal 2000. The acquired in-process technology represents the appraised value of technologies in the development stage that had not yet reached technological feasibility and does not have alternative future uses.

In January 1999, we acquired certain assets of MI Acquisition LLP, for a total purchase price of $6.8 million. The purchase price allocation, based on an independent appraisal, resulted in a $3.6 million charge to research and development in the fourth quarter of fiscal 1999 for acquired in-process technology. The acquired in-process technology represents the appraised value of technology in the development stage that had not yet reached technological feasibility and does not have alternative future uses.

In addition to the transactions described above, we purchased businesses in smaller transactions. The total amount allocated to goodwill and identified intangibles for these transactions was $15.4 million in fiscal 2001 ($2 million in fiscal 2000), which represents a substantial majority of the consideration for these transactions.

The unaudited pro forma information below assumes that companies acquired in fiscal 2001 and 2000 had been acquired in at the beginning of fiscal 2000 and includes the effect of amortization of goodwill and other identified intangibles from that date. The impact of charges for in process research and development has been excluded. This is presented for informational purposes only

and is not indicative of the results of future operations or results that would have been achieved had the acquisitions taken place at the beginning of fiscal 2000.

IN THOUSANDS, EXCEPT PER SHARE AMOUNTS (UNAUDITED)	YEARS ENDED MARCH 31, 2001	2000
Net revenues	$ 1,660,019	$ 1,021,738
Net income	24,143	639,927
Basic earnings per share	$ 0.07	$ 2.00
Diluted earnings per share	$ 0.07	$ 1.85

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Report of Ernst & Young LLP, Independent Auditors

The Board of Directors and Stockholders

Xilinx, Inc.

We have audited the accompanying consolidated balance sheets of Xilinx, Inc. as of March 31, 2001 and 2000, and the related consolidated statements of income, stockholders' equity and cash flows for each of the three years in the period ended March 31, 2001. Our audits also included the financial statement schedule listed in the Index at Item 14(a). These financial statements and schedule are the responsibility of the Company's management. Our responsibility is to express an opinion on these financial statements and schedule based on our audits.

We conducted our audits in accordance with auditing standards generally accepted in the United States. Those standards require that we plan and perform the audit to obtain reasonable assurance about whether the financial statements are free of material misstatement. An audit includes examining, on a test basis, evidence supporting the amounts and disclosures in the financial statements. An audit also includes assessing the accounting principles used and significant estimates made by management, as well as evaluating the overall financial statement presentation. We believe that our audits provide a reasonable basis for our opinion.

In our opinion, the consolidated financial statements referred to above present fairly, in all material respects, the consolidated financial position of Xilinx, Inc. at March 31, 2001 and 2000, and the consolidated results of its operations and its cash flows for each of the three years in the period ended March 31, 2001, in conformity with accounting principles generally accepted in the United States. Also, in our opinion, the related financial statement schedule, when considered in relation to the basic financial statements taken as a whole, presents fairly in all material respects the information set forth therein.

As discussed in Notes 2 and 3 to the consolidated financial statements, in the fiscal year ended March 31, 1999, the Company changed its method of recognizing revenue on certain shipments to its distributors.

Ernst & Young LLP

San Jose, California
April 18, 2001, except for
the first paragraph of Note 12 as to which
the date is May 10, 2001

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Schedule II: Valuation and Qualifying Accounts

(IN THOUSANDS) DESCRIPTION	BEGINNING OF YEAR	CHARGED TO INCOME	DEDUCTIONS (A)	BALANCE AT END OF YEAR
For the year ended March 31, 1999				
Allowance for doubtful accounts:	$ 3,524	$ 23	–	$ 3,547
price adjustments and customer returns:	$ 4,884	$ 2,106	$ 3,128	$ 3,862
For the year ended March 31, 2000				
Allowance for doubtful accounts:	$ 3,547	$ 35	$ 9	$ 3,573
price adjustments and customer returns:	$ 3,862	$ 13,950	$ 5,846	$ 11,966
For the year ended March 31, 2001				
Allowance for doubtful accounts:	$ 3,573	$ 60	$ 8	$ 3,625
price adjustments and customer returns:	$ 11,966	$ (7,894)	$ 161	$ 3,911

(a) Represents amounts written off against the allowance, customer returns or pricing adjustments to international distributors.

SUPPLEMENTARY FINANCIAL DATA

Quarterly Data (Unaudited)

(IN THOUSANDS EXCEPT PER SHARE AMOUNTS) YEAR ENDED MARCH 31, 2001	FIRST QUARTER	SECOND QUARTER	THIRD QUARTER	FOURTH QUARTER
Net revenues	$ 364,875	$ 437,360	$ 450,103	$ 407,020
Gross margin	227,946	269,035	270,904	212,071
Net income	93,826	114,056	(10,507)#	(162,117)±
Net income per share:				
Basic	$ 0.29	$ 0.35	$ (0.03)	$ (0.49)±
Diluted	$ 0.27	$ 0.32	$ (0.03)	$ (0.49)±
Shares used in per share calculations:				
Basic	326,030	329,650	329,643	330,682
Diluted	353,448	356,046	329,643	330,682

± Net income includes a pre-tax write down of $362,124 capital loss from the UMC investment.

Net income includes pre-tax in process R&D write off of $90,700 in connection with RocketChips acquisition.

± and # Net income also includes pre-tax amortization of acquisition related items including goodwill, other intangibles, and deferred compensation of $9.6 million and $12.8 million in the third quarter and fourth quarter, respectively.

(IN THOUSANDS EXCEPT PER SHARE AMOUNTS) YEAR ENDED MARCH 31, 2000	FIRST QUARTER	SECOND QUARTER	THIRD QUARTER	FOURTH QUARTER
Net revenues	$ 211,403	$ 238,762	$ 264,259	$ 306,569
Gross margin	131,645	148,557	164,683	192,070
Net income	51,615	55,974	68,504	476,357±
Net income per share:				
Basic	$ 0.16	$ 0.18	$ 0.21	$ 1.47±
Diluted	$ 0.15	$ 0.16	$ 0.20	$ 1.36±
Shares used in per share calculations:				
Basic	313,865	317,534	319,891	323,397
Diluted	336,825	343,007	346,162	351,461

± Net income includes a $398,089 capital gain (net of taxes) from the UMC/USIC merger, or $1.23 per basic share and $1.13 per diluted share.

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Item 9. Changes In and Disagreements with Accountants on Accounting and Financial Disclosure

Not applicable

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Item 10. Directors and Executive Officers of the Registrant

Certain information required by Part III is omitted from this Report in that the Registrant will file a definitive proxy statement pursuant to Regulation 14A (the Proxy Statement) not later than 120 days after the end of the fiscal year covered by this Report, and certain information included therein is incorporated herein by reference. Only those sections of the Proxy Statement which specifically address the items set forth herein are incorporated by reference. Such incorporation does not include the Compensation Committee Report or the Performance Graph included in the Proxy Statement.

The information concerning the Company's directors required by this Item is incorporated by reference to the Company's Proxy Statement.

The information concerning the Company's executive officers required by this Item is incorporated by reference to the section in Item 1 hereof entitled "Executive Officers of the Registrant."

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Item 11. Executive Compensation

The information required by this Item is incorporated by reference to the Company's Proxy Statement.

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Item 12. Security Ownership of Certain Beneficial Owners and Management

The information required by this Item is incorporated by reference to the Company's Proxy Statement.

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Item 13. Certain Relationships and Related Transactions

The information required by this Item is incorporated by reference to the Company's Proxy Statement.

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Item 14. Exhibits, Financial Statement Schedules and Reports on Form 8-K

(a) (1) The Financial Statements required by Item 14 (a) are filed as Item 8 of this annual report.

(2) The Financial Statement Schedule required by Item 14 (a) is filed as Item 8 of this annual report.

Schedules not filed have been omitted because they are not applicable, are not required or the information required to be set forth therein is included in the financial statements or notes thereto.

(3) The exhibits listed below in (c) are filed or incorporated by reference as part of this annual report.

(b) Reports on Form 8-K. No reports on Form 8-K were filed during the fourth quarter of fiscal 2001.

(c) Exhibit

EXHIBIT NUMBER	DESCRIPTION
3.1 (1)	Restated Certificate of Incorporation of the Company, as amended to date.
3.2 (2)	Bylaws of the Company, as amended to date.
4.1 (3)	Preferred Shares Rights Agreement dated as of October 4, 1991 between the Company and The First National Bank of Boston, as Rights Agent.
10.1 (4)	Lease dated March 27, 1995 for adjacent facilities at 2055 Logic Drive and 2065 Logic Drive, San Jose, California.
10.2 (4)	First Amendment to Master Lease dated April 27, 1995 for the Company's facilities at 2100 Logic Drive and 2101 Logic Drive, San Jose, California.
10.3 (5)	Lease dated October 8, 1997 for an additional facility on Logic Drive, San Jose, California.
10.4.1 (6)	Agreement of Purchase and Sale of Land in Longmont Colorado, dated November 24, 1997.
10.4.2 (6)	First Amendment to Agreement of Purchase and Sale of Land in Longmont Colorado, dated January 15, 1998.
10.5 (2)	1988 Stock Option Plan, as amended.
10.6 (7)	1990 Employee Qualified Stock Purchase Plan, as amended.
10.7 (7)	1997 Stock Option Plan.
10.8 (2)	Form of Indemnification Agreement between the Company and its officers and directors.
10.9 (8)	Letter Agreement dated as of January 22, 1996 of the Company to Willem P. Roelandts.
10.10.1 (8)	Consulting Agreement dated as of June 1, 1996 between the Company and Bernard V. Vonderschmitt.
10.10.2 (6)	Amended Services and Compensation Exhibit to the Consulting Agreement dated as of June 1, 1996 between the Company and Bernard Vonderschmitt.
10.10.3 (6)	Second Amendment to the Consulting Agreement dated as of June 1, 1996 between the Company and Bernard Vonderschmitt.
10.11 (9)	Letter Agreement dated as of April 1, 1997 of the Company to Richard W. Sevcik.
10.12.1 (10) (11)	Foundry Venture Agreement dated as of September 14, 1995 between the Company and United Microelectronics Corporation (UMC).
10.12.2 (10) (11)	Fabven Foundry Capacity Agreement dated as of September 14, 1995 between the Company and UMC.
10.12.3 (10) (11)	Written Assurances Re Foundry Venture Agreement dated as of September 29, 1995 between UMC and the Company.
10.13.1 (8) (10)	Advance Payment Agreement entered into on May 17, 1996 between Seiko Epson Corporation and the Company.
10.13.2 (6) (10)	Amended and Restated Advance Payment Agreement with Seiko Epson dated December 12, 1997.
10.14 (8)	Indenture dated November 1, 1995 between the Company and State Street Bank and Trust Company.
10.15 (10) (12)	Letter Agreement dated January 13, 2000 between the Company and UMC.
21.1	Subsidiaries of the Company.
23	Consent of Ernst & Young LLP, Independent Auditors.
24.1	Power of Attorney.

(1) Filed as an exhibit to the Company's Annual Report on Form 10-K for the fiscal year ended March 30, 1991.
(2) Filed as an exhibit to the Company's Registration Statement on Form S-1 (File No. 33-34568) which was Declared effective June 11, 1990.
(3) Filed as an exhibit to the Company's Registration Statement on Form S-1 (File No. 33-43793) effective November 26, 1991.
(4) Filed as an exhibit to the Company's Quarterly Report on Form 10-Q for the quarter ended April 1, 1995.
(5) Filed as an exhibit to the Company's Quarterly Report on Form 10-Q for the quarter ended September 27, 1997.
(6) Filed as an exhibit to the Company's Quarterly Report on Form 10-Q for the quarter ended December 27, 1997.
(7) Filed as an exhibit to the Company's Registration Statement on Form S-8 (File No. 333-62897) effective September 4, 1998.
(8) Filed as an exhibit to the Company's Annual Report on Form 10-K for the fiscal year ended March 30, 1996.
(9) Filed as an exhibit to the Company's Annual Report on Form 10-K for the fiscal year ended March 29, 1997.
(10) Confidential treatment requested as to certain portions of these documents.
(11) Filed as an exhibit to the Company's Quarterly Report on Form 10-Q for the quarter ended September 30, 1995.
(12) Filed as an exhibit to the Company's Annual Report on Form 10-K for the fiscal year ended March 31, 2001.

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Signatures

Pursuant to the requirements of Section 13 or 15(d) of the Securities Exchange Act of 1934, the Registrant, has duly caused this Annual Report to be signed on its behalf by the undersigned, thereunto duly authorized, in the City of San Jose, State of California, on the 7th day of June, 2001.

XILINX, INC.

By: /s/ Willem P. Roelandts

Willem P. Roelandts,
Chief Executive Officer and President

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Exhibit 21.1: Subsidiaries of Registrant

NAME	PLACE OF INCORPORATION OR ORGANIZATION
Xilinx, Ltd.	United Kingdom
Xilinx, K.K.	Japan
Xilinx Development Corporation	California, U.S.A.
Xilinx International, Inc.	Colorado, U.S.A.
Xilinx, SARL	France
Xilinx, GmbH	Germany
Xilinx AB	Sweden
Xilinx Benelux, Bvba	Belgium
Xilinx Holding One Limited	Ireland
Xilinx Holding Two Limited	Ireland
Xilinx Holding Three Ltd.	Cayman Islands
Xilinx Holding Four Limited	Cayman Islands
Xilinx Ireland	Ireland
Xilinx Antilles N.V.	Netherlands Antilles
Xilinx Netherlands B.V.	Netherlands

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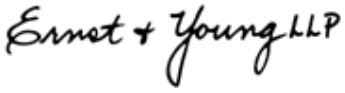
Exhibit 23: Consent of Ernst & Young LLP, Independent Auditors

We consent to the incorporation by reference in the Registration Statement (Form S-8 Nos. 33-80075, 33-83036, 33-52184, 33-67808, 333-44233, 333-62897, 333-51510) pertaining to the 1988 Stock Option Plan, the 1997 Stock Plan and the 1990 Employee Qualified Stock Purchase Plan of Xilinx, Inc., the 1996 Stock Option Plan, the 1996 Director Stock Option Plan, the 2000 Non-Qualified Stock Option Plan, and the 2000 Equity Incentive Stock Option Plan of Rocketchips, Inc., and the Non-Qualified Stock Option Agreement for Paul M. Russo; and (Form S-3 No. 333-51514) of our report dated April 18, 2001 (except for the first paragraph of Note 12, as to which the date is May 10, 2001), with respect to the consolidated financial statements and schedule of Xilinx, Inc. included in the Annual Report (Form 10-K) for the year ended March 31, 2001.



San Jose, California
June 8, 2001

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Exhibit 24.1: Power of Attorney

KNOW ALL PERSONS BY THESE PRESENTS, that each person whose signature appears below constitutes and appoints Willem P. Roelandts and Kris Chellam, jointly and severally, his attorneys-in-fact, each with the power of substitution, for him in any and all capacities, to sign any amendments to this Report on Form 10-K, and to file the same, with exhibits thereto and other documents in connection therewith, with the Securities and Exchange Commission, hereby ratifying and confirming all that each of said attorneys-in-fact, or his substitute or substitutes, may do or cause to be done by virtue hereof.

Pursuant to the requirements of the Securities Exchange Act of 1934 this Report on Form 10-K has been signed below by the following persons on behalf of the Registrant in the capacities and on the dates indicated.

SIGNATURE	TITLE	DATE
BERNARD V. VONDERSCHMITT (Bernard V. Vonderschmitt)	Chairman of the Board	June 7, 2001
WILLEM P. ROELANDTS (Willem P. Roelandts)	President and Chief Executive Officer (Principal Executive Officer)	June 7, 2001
KRIS CHELLAM (Kris Chellam)	Senior Vice President, Finance and Chief Financial Officer (Principal Accounting and Financial Officer)	June 7, 2001
DENNIS SEGERS (Dennis Segers)	Senior Vice President and General Manager, Advanced Products Group	June 7, 2001
RICHARD W. SEVCIK (Richard W. Sevcik)	Senior Vice President, IP, Services and Software Group	June 7, 2001
JOHN L. DOYLE (John L. Doyle)	Director	June 7, 2001
JERALD G. FISHMAN (Jerald G. Fishman)	Director	June 7, 2001
PHILIP T. GIANOS (Philip T. Gianos)	Director	June 7, 2001
WILLIAM G. HOWARD, JR. (William G. Howard, Jr.)	Director	June 7, 2001
FRANK SEIJI SANDA (Frank Seiji Sanda)	Director	June 7, 2001
ELIZABETH VANDERSLICE (Elizabeth Vanderslice)	Director	June 7, 2001

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