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Danny Biran
Sr. VP, Product & Corporate Marketing

Forward-Looking Statements

Statements in this presentation that are not historical are "forward-looking statements" as the term is defined in the Private Securities Litigation Reform Act of 1995. Forward-looking statements are generally written in the future tense and/or preceded by words such as "will", "expects", "anticipates", or other words that imply or predict a future state. Forward-looking statements include any projection of competitive dynamics, future competitive position and sales growth prospects, CPLD or FPGA product mix or growth, PLD usage, logic density or logic element growth, die area reduction, power consumption projections, device performance characteristics, changes in price per function, ASIC design characteristics, revenue, gross margin, OPEX spending or other financial items discussed in this presentation as well as comments relating to new products, expected 40-nm shipment timing, anticipated product rollout schedules, intentions to secure financing, and share repurchase plans. Investors are cautioned that all forward-looking statements in this presentation involve risks and uncertainty that can cause actual results to differ from those currently anticipated, due to a number of factors, including without limitation, customer business environment, vertical market mix, market acceptance of the company's products, the rate of growth of the company's new products including the Stratix® IV, Arria® GX, Cyclone® III, Stratix III, Stratix II, MAX® II and HardCopy® device families, changes in the mix of our business between prototyping and production-based demand, the continuance of suitable financial market conditions, as well as changes in economic conditions, the company's share price, share repurchases, and other risk factors discussed in documents filed by the company with the Securities and Exchange Commission from time to time. Copies of Altera's SEC filings are posted on the company's web site and are available from the company without charge. Forward-looking statements are made as of the date of this presentation, and, except as required by law, the company does not undertake an obligation to update its forward-looking statements to reflect future events or circumstances.

Financial Framework



Growth



Efficiency



Shareholder Value

----- **2Q08 Results** -----

13%
growth
vs. 2Q07

32%
Operating
Margin

\$98M
Net Income
& 31% ROE

ASIC % Design Starts by Technology

↑ Integration, Lower Cost, Performance	Process Node	2002 %	2003 %	2004 %	2005 %	2006 %	2007 %	2008 %	2009 %	2010 %	2011 %	Dev. Costs \$M	↑ Increased Risks & Development Cost
	0.022 μm	0	0	0	0	0	0	0	0	0	0	110	
	0.032 μm	0	0	0	0	0	0	0	1	ALTERA	ALTERA	80	
	0.040 μm	0	0	0	0	0	1	ALTERA	ALTERA	6	7	60	
	0.045 μm	0	0	0	0	0	1	2	4	6	7	60	
	0.065 μm	0	0	0	1	2	ALTERA	8	10	13	15	55	
	0.09 μm	0	1	8	ALTERA	ALTERA	23	23	24	24	24	30	
	0.13 μm	ALTERA	ALTERA	ALTERA	29	29	27	27	25	24	24	20	
	0.18 μm	38	27	23	20	17	14	12	10	10	8	13	
	0.25 μm	16	15	12	12	11	9	9	8	7	6	5	
	0.35 μm	21	16	12	12	11	10	8	8	6	5	3	
	0.5 μm	5	4	3	7	7	6	6	5	4	4	2	
L>0.5 μm	1	1	0	6	6	6	5	5	5	5	<1		
Total	100	100	100	100	100	100	100	100	100	100	100		

#1 ASIC Design Technology

#1 PLD Design Technology ALTERA

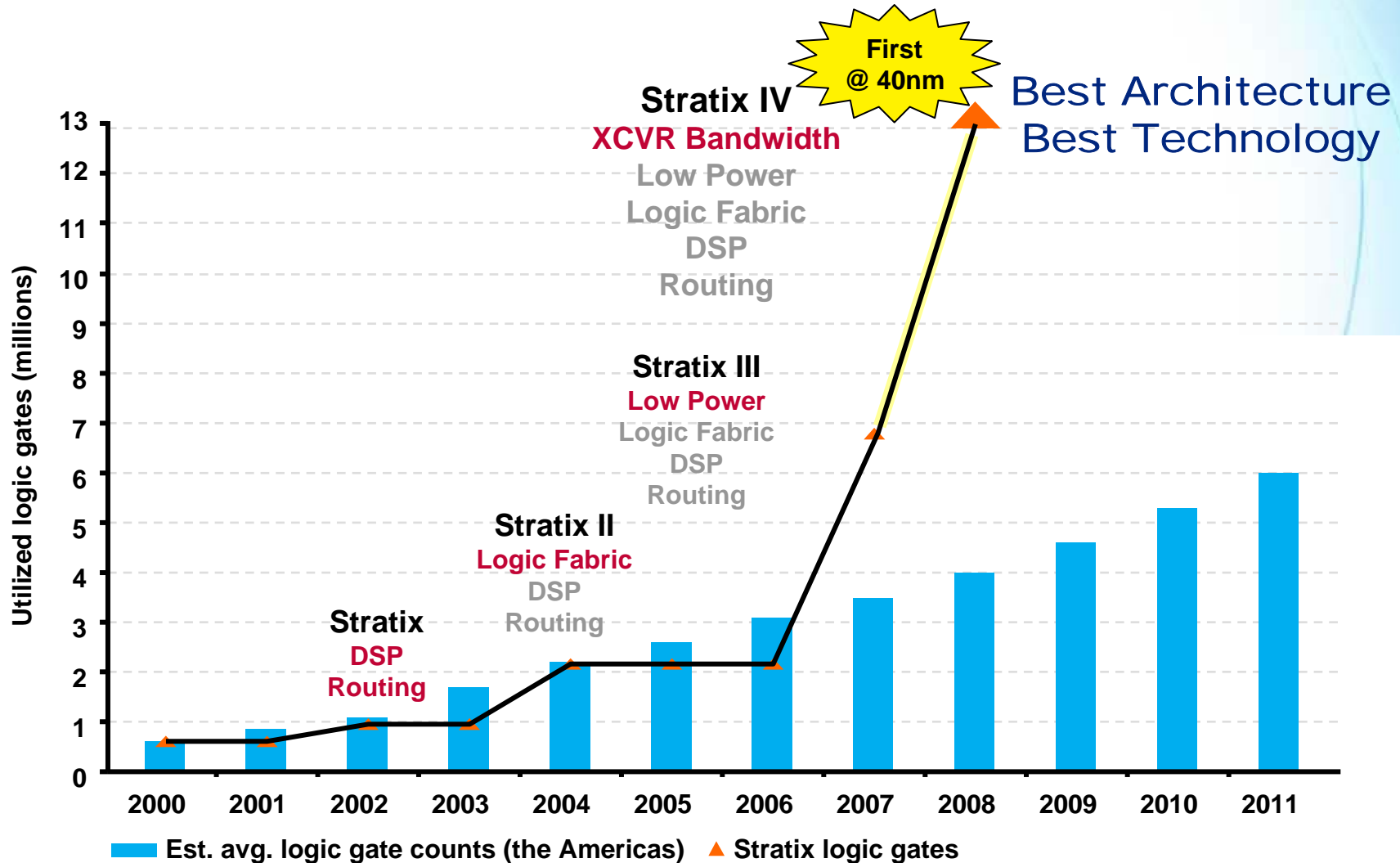
Source: Altera & Gartner Nov 07

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Stratix Key Innovations & Average ASIC Density



Note: Data based on Gartner Dataquest report 11/21/07

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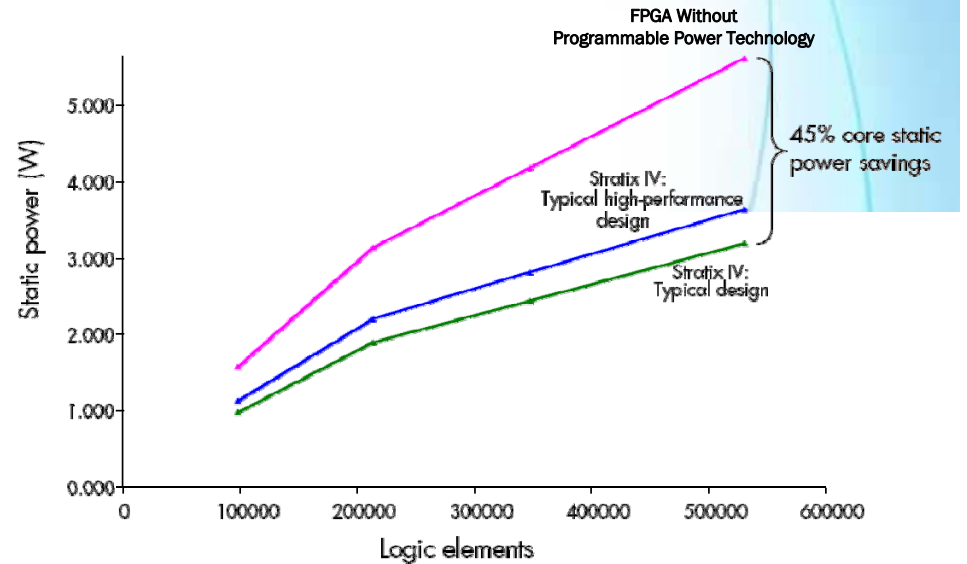
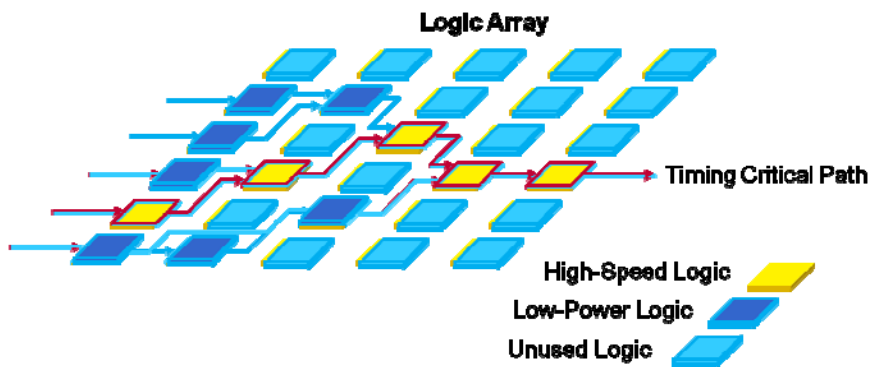
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Stratix IV Low Power Advantage

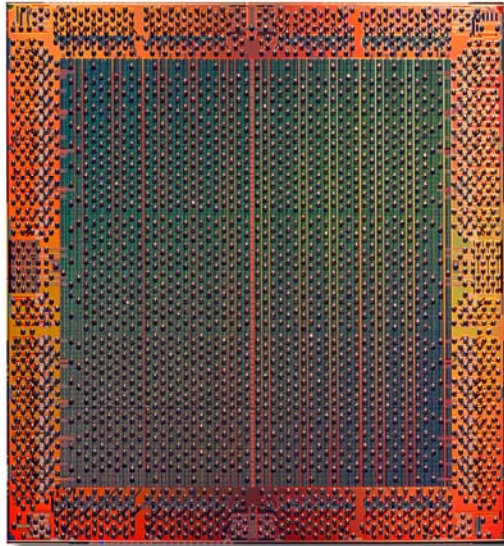
Programmable Power Technology

Programmable Power Technology Advantages Proven in Stratix III

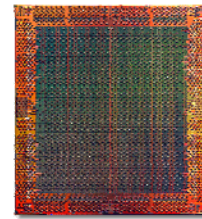
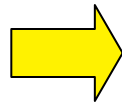


Results Automated for the Designer via Quartus II PowerPlay Technology

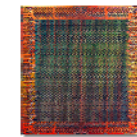
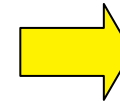
Reaching the Tipping Point



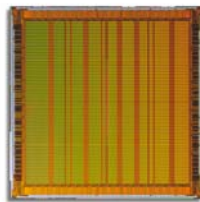
**130nm FPGA
(Stratix)**



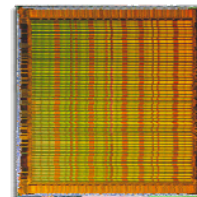
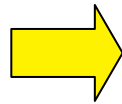
**40nm FPGA
(Stratix IV)**



**40nm ASIC
(HardCopy IV)**



130nm ASIC



130nm ASIC

Relative die size estimates based on design of approximately 4M logic gates and 8M bits of RAM

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Reaching the Tipping Point

	130nm ASIC	40nm FPGA
I/O High Speed Serial I/O (HSSI) Low Voltage Diff. Signaling (LVDS)	3.125 Gbps 1.0 Gbps	8.5 Gbps 1.5 Gbps
External Memory Interface DDR3 clock rate DDR2 clock rate	266 MHz 233 MHz	533 MHz 400 MHz
Core System clock rate Memory clock rate	350 MHz 600 MHz	350 MHz 600 MHz

Superior I/O Speed for Enhanced Bandwidth

ASIC data based on product documentation & datasheets from ASIC Suppliers

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Reaching the Tipping Point

	130nm ASIC	40nm FPGA
Sample Protocol Support		
PCI Express Gen 1	●	●
Fibre Channel 1, 2	●	●
Serial RapidI/O	●	●
Gigabit Ethernet, XAUI, HiGig+	●	●
OC-3/12/48	●	●
PCI Express Gen 2	○	●
Fibre Channel 4	○	●
SATA	○	●
SAS	○	●
CEI 6G	○	●

*40nm FPGA Provides Comprehensive Support
for Next Generation Systems*

ASIC data based on product documentation & datasheets from ASIC Suppliers

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Stratix IV & HardCopy IV Overview

- Altera is first with 40-nm FPGAs
 - FPGAs with >2.5 billion transistors
 - Over 500 Customers in Early Adopter Program
- Stratix IV devices sweep the high-end FPGA scorecard



Selection criteria	Stratix IV advantage
Density	>2X larger
Transceiver bandwidth	>2X bandwidth (48 XCVRs up to 8.5 Gbps)
Performance	>2 speed grade advantage (35%)
Memory interface	33% to 60% faster (1067 Mbps)
Power	1/2 power

- HardCopy IV ASICs: now featuring high-speed transceivers
- Quartus II software v8.0: #1 performance/productivity
 - Available since June 2008