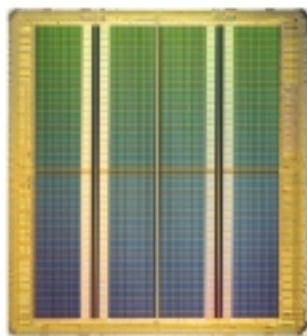


System-on-a-  
Programmable-Chip  
Solutions



**2 0 0 1**  
**ANNUAL REPORT**

**ALTERA®**

## Corporate Profile

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Altera Corporation, The Programmable Solutions Company®, is a world leader in one of the fastest growing segments of the semiconductor industry: high-density programmable logic devices (PLDs). Altera PLDs are standard integrated circuits that offer significant advantages over custom logic chips such as application-specific integrated circuits (ASICs). Today's high-density PLDs, used in concert with Altera's desktop software design tools and optimized intellectual property building blocks, allow electronic systems manufacturers to execute on a single chip the same functionality that previously consumed an entire printed circuit board. This methodology, called "system on a programmable chip" (SOPC), helps electronic systems manufacturers shorten time-to-market and reduce development costs.

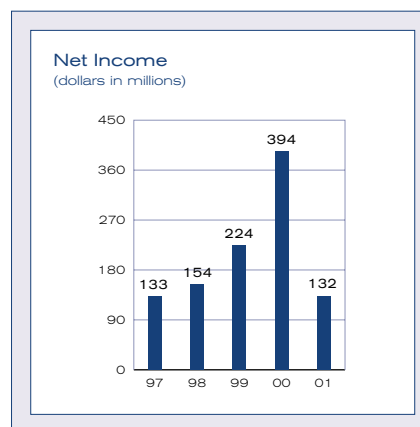
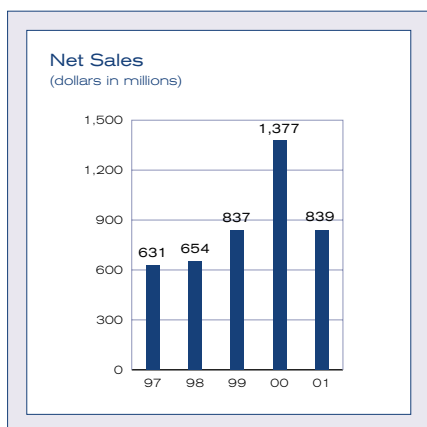
Altera serves over 14,000 customers in four primary market segments: communications, electronic data processing, industrial, and consumer applications. The company sells its chips worldwide and derives more than half of its revenues from markets outside the United States. Altera common stock is traded on The Nasdaq Stock Market under the symbol ALTR. Altera's web site is located at <http://www.altera.com>.

## Financial Highlights

### Years ended December 31,

(In thousands, except per share amounts)

	1997	1998	1999	2000	2001
Net sales	\$ 631,114	\$ 654,342	\$ 836,623	\$1,376,815	\$ 839,376
Net income <i>(See Notes 1, 2)</i>	133,453	154,387	223,994	394,122	132,406
Diluted net income per share <i>(See Notes 1, 2)</i>	0.34	0.39	0.54	0.95	0.33
Income from operations <i>(See Note 2)</i>	226,955	231,843	306,022	521,164	148,976
Total research and development expenses	54,417	59,864	86,065	178,678	170,869
Capital expenditures	80,879	23,950	29,821	87,508	65,758
Cash and short-term investments	377,569	579,106	845,666	1,133,609	805,691
Stockholders' equity	536,687	881,721	1,118,073	1,247,930	1,114,500



(See Notes 1, 2)

#### Notes

The company provides pro forma financial data as an alternative for understanding its operating results. These measures are not in accordance with Generally Accepted Accounting Principles ("GAAP"), and may be different from pro forma measures used by other companies. For details on GAAP results, refer to Selected Consolidated Financial Data on page 8. Pro forma results reflected on this page and the corresponding charts on page 2 and 4 exclude the following:

1. Excludes the one-time gain and other one-time charges and credits of \$174.0 million relating to the sale of the company's interest in WaferTech, LLC in 2000.
2. Excludes the effects of the inventory charges of \$154.5 million and restructuring and other special charges of \$47.7 million taken during 2001.

## Letter to Shareholders

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The year 2001 was extraordinarily challenging for the semiconductor industry and for Altera. Following a year of robust growth, 2001 marked the sharpest decline ever experienced in semiconductor industry revenues. Altera's revenues for 2001 were \$839 million, down 39 percent from the prior year. Income on a pro forma basis was \$132 million, \$0.33 per diluted share.

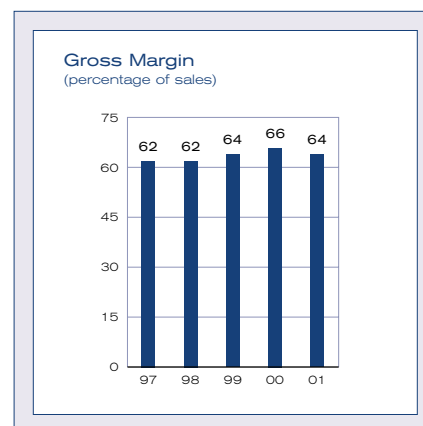
The year began with slowing sales due to a North American inventory correction that started in late 2000. By the first quarter of 2001, customer end demand in many of Altera's North American markets had begun to contract, further reducing demand for Altera's products. As the year progressed, economic conditions weakened worldwide, extending the negative impact on the company. Overall, North America saw the most severe change in revenues as sales declined 52 percent from 2000 levels due to recessionary economic conditions and high levels of customer inventory. While all our markets contracted, the greatest change occurred in the communications market, where revenue declined 47 percent. The fourth quarter appears to be the bottom of this cyclical downturn, as customers began to order products to replace depleted inventory, leading to improved customer backlog and a favorable ratio of incoming orders to sales.

As a result of the dramatic change in business environment, from exceptionally strong growth in 2000 to the sharp contraction in 2001, and despite severely reduced wafer procurement, Altera's inventories grew well beyond levels seen in earlier contractions. The company booked its first material inventory write-downs and has revised its inventory model going forward to shift more of the company's demand to a build-to-order basis. In addition, newer products will rely on

more flexible die bank inventory so that, in the future, the company can hold less inventory without sacrificing customer delivery performance.

This rapid change in business conditions also required that Altera curtail discretionary spending and implement several cost reduction and restructuring measures. We were able to reduce overhead and infrastructure costs without jeopardizing our development momentum and sales presence. Charges associated with these restructuring activities and the inventory write-downs more than offset the ongoing profits of the company, leading to a net loss for the year of \$39.8 million, \$0.10 per diluted share.

On a pro forma basis (excluding the inventory write-downs), gross margins were 63.8 percent of revenue—a good showing for a semiconductor manufacturer in any year, and an unusually strong result in a year of revenue declines. In such a difficult year, this performance demonstrates the benefits of Altera's fabless business model, which delivers strong gross margins throughout the business cycle.



(See Note 2 on page 1)

We invested aggressively in new technology in 2001. R&D spending of \$171 million was similar to the prior year, and with this continuing commitment, Altera is well positioned to drive top-line growth in the coming years as industry conditions improve. SG&A spending has dropped steadily during the year. The company's SG&A spending in the fourth quarter was 23 percent below our peak spending in the first quarter of 2001. Pro forma operating income for the year was 17.7 percent of revenue, well below our long-term expectations for the company. Altera's balance sheet remained strong and debt-free, with a cash position of \$806 million. As part of the company's ongoing share repurchase program, during 2001 Altera repurchased 7.2 million shares of the company's stock at a cost of \$183 million. Since the beginning of this program in 1996, Altera has returned \$890 million to shareholders through share repurchases.

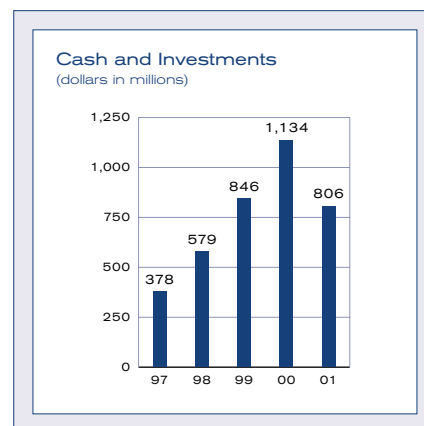
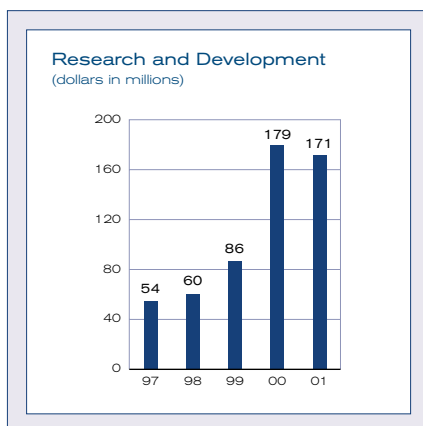
Despite the operating difficulties, the company reached several new milestones this year. Most importantly, we became more competitive across all dimensions of our business. The increased R&D investments of the past several years are paying off, and customers now take advantage

of Altera system-on-a-programmable-chip (SOPC) solutions to address more of their design needs. New product sales grew, with the greatest gains in the APEX™ 20KE family, an advanced field-programmable gate array (FPGA) device family. Total FPGA-based product revenues were \$477 million in 2001. Sales of complex programmable logic devices (CPLDs), composed of the Classic™ and MAX® families, were \$299 million, and we widened our CPLD market share lead in 2001.

The revenue potential from new design wins increased sharply during the year, setting new records. This performance demonstrates the power of the company's growing range of products, which capitalize on Altera's pioneering first-to-market breakthroughs, more powerful intellectual property offerings, and higher levels of software performance. These design wins set the stage for future growth as they enter production.

### Integrated Product Portfolio

Altera's new products and our SOPC capability enable our customers to use programmable logic across a much wider variety of applications. Our goal is to provide more SOPC value to our



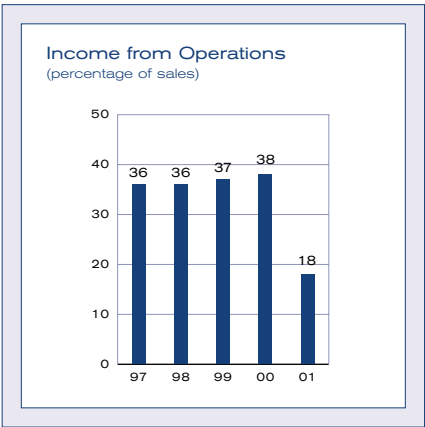
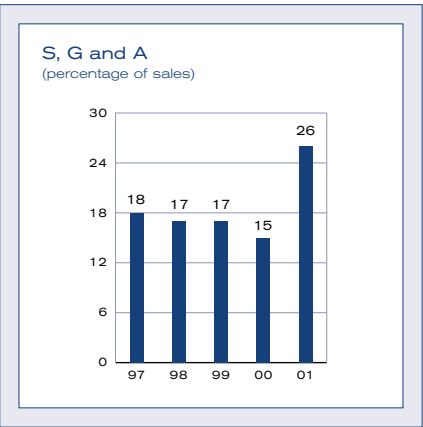
customers through a comprehensive and integrated series of products that leverages advanced Altera programmable logic technology.

Through the new products we introduced in 2001, we have taken major steps to deliver increased SOPC value, and we lead the industry with innovative first-to-market products. The APEX 20KC devices, introduced during 2001, were the first devices to offer the performance benefits of all-copper interconnect. Extending the leadership established in 2000 with Nios™ processor-based Excalibur™ solutions, the first custom-designed soft microcontroller in a PLD, Altera's Excalibur solutions now include an ARM9™ embedded microprocessor integrated within a programmable device. Altera is the first major PLD company to offer this capability to customers. Altera also introduced Mercury™ devices, the first programmable ASSPs that combine a high-speed transceiver and programmable logic, and HardCopy™ devices, the first to offer a low-cost migration path for high-density designs transitioning from prototype to production. Altera's high-density APEX II family, built for the data path with its unique fast and flexible I/O features, also began shipping. The newest APEX II devices have become the

first PLDs utilizing advanced 0.13-micron process technology. These product introductions helped Altera solidify our position as a leader in the semiconductor industry.

Altera's core competency remains firmly rooted in programmable logic, and the distinctive value created by these new products rests in their programmable capability. These new products each offer distinctive features and complement each other in numerous ways, making Altera that much more attractive to customers. For example, a high-density APEX II device or Excalibur embedded processor solution becomes even more valuable to a customer because of the presence of a low-cost HardCopy migration path. In another case, a Mercury customer can take advantage of easy APEX II integration and use an APEX II device with its data path focused performance as part of an overall design. It is these types of synergies that make Altera's product range so attractive.

Software advantages are as important to our customers as new silicon capabilities. Tens of thousands of system designers around the world use the company's development software.



(See Note 2 on page 1)

The unmatched breadth of Altera's MegaCore® intellectual property (IP) offerings and third-party IP cores gives Altera customers even more flexibility. Separate IP cores can be combined at a system level using Altera software tools and development kits, easing complex system integration.

### The Next Step

Altera innovations are part of a long-held strategy to develop PLDs that customers use to create SOPC solutions. Altera has led the industry at every step as PLDs have evolved from simple glue logic to fully system-capable devices. Altera's continued SOPC-driven innovation means that Altera products will continue to displace other silicon-based solutions.

The newly introduced Stratix™ family takes SOPC potential to new levels. Stratix devices employ a new architecture that was created to address rapidly expanding system complexity. Stratix devices are equipped with the industry's first programmable digital signal processing (DSP) blocks, making the devices well suited for a wide variety of computation-intensive applications. Additionally, the unique Stratix architecture delivers more bandwidth, logic, and memory than any previous Altera PLD, offering customers additional flexibility and up to twice the performance while simplifying the design process. The Stratix architecture was also designed to facilitate the development of future Stratix products, which will shorten Altera product development cycles and reduce future development costs. Customers are already benefiting from the advantages of Stratix devices as they design with the February 2002 Quartus® II software release, and their interest in the Stratix architecture has been extremely encouraging.

## Stratix Devices

Altera ushers in a new era for programmable logic with the introduction of the Stratix device family, the industry's fastest, most powerful PLDs. Building on a long history of innovation, Altera is once again delivering the fastest devices in the industry and achieving the highest levels of integration with the most memory, logic elements, and DSP functionality ever in a PLD.

The Stratix architecture is a result of intense customer input. Architectural innovations allowed Altera to address our customers' needs for more processing power, speed, functionality, and cost efficiencies. This revolutionary family streamlines the customers' design process to speed time-to-market despite significantly increased device complexity.

Altera has simplified the design process by enabling a true timing-locked block-based design methodology. For the first time ever, a designer, or teams of designers, can work on specific areas of a design and lock in the timing integrity to break the endless loop of re-optimization during integration. The powerful combination of our Stratix devices and Quartus II design software allows design teams to shorten their design cycles and increase overall system performance by as much as 100%.

Altera is committed to deliver the best, most innovative solutions to our customers, and the new Stratix device family is the next step. Using Stratix devices and Quartus II software, Altera customers can focus on their core competencies and speed their products to market with greater cost-efficiency and less risk.

## HardCopy Devices

Product development teams today face uncertainty, high development costs, resource constraints, and time-to-market pressure when considering conversion from a high-density PLD to an ASIC. Altera's HardCopy devices offer a new solution, unique in the market, that extends the flexibility, power, and time-to-market advantages of PLDs to the more cost-sensitive applications traditionally served by ASICs.

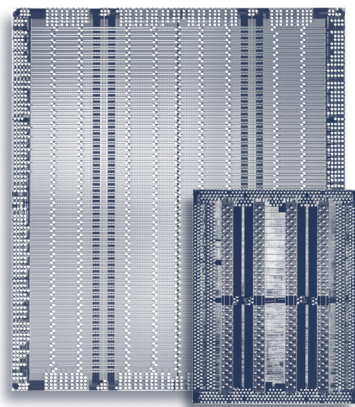
HardCopy devices provide a low-risk, cost-effective, time-saving alternative to ASICs for high-volume production. Through a combination of proprietary silicon design and an automated conversion process, Altera helps customers move seamlessly from a programmable solution to a low-cost, custom implementation of their designs. Using competitively priced HardCopy devices, product development teams can enjoy the benefits of a shorter development time and enter the market earlier, while creating a cost-effective solution for volume production.

Customers using HardCopy devices save money, time, and resources, all with no risk. Together, these advantages result in a cost of ownership that no ASIC conversion can match.

### Actual Die Size Reduction

The die size for a HardCopy device is up to 70% smaller than the die size of the equivalent PLD, allowing a significantly lower unit cost.

APEX 20KE EP20K1500E



HardCopy  
HC20K1500E

## The Potential

Altera is changing the competitive landscape in the semiconductor industry. Altera PLDs are becoming more attractive to customers because of their SOPC capability, while at the same time they are uniquely suited to take advantage of the economics of increasingly advanced process geometries. As the front-end costs to develop new-generation chips climb exponentially, large revenue streams will be required to recover these costs. Fewer and fewer customers will have the volume potential to justify an advanced ASIC design, and ASSP vendors will struggle to create standard parts that will support the necessary volumes. The PLD model, on the other hand, spreads the costs of developing advanced technology across a large number of customers who use the product for a wide range of customer-specific applications. This approach makes programmable logic an even more attractive path to access the advantages of the most advanced processes. The convergence of these realities and Altera's SOPC strategy provides fertile ground for future growth.

With design win momentum in 2001 and the introduction of new standard setting products, we have significantly increased our growth potential. Our new product pipeline is full, and 2002 will bring additional revolutionary products that deliver more performance for even the most demanding SOPC applications. We are still at the beginning stage of expanding the application space for PLDs. With our broad product portfolio, our expanding ability to address new applications, and our time-to-market advantages, we have a great opportunity to capture market share from other semiconductor alternatives.

### Special Thanks

We asked a lot of our people this year, and they deserve special thanks. They have remained resilient and dedicated to delivering the advanced Altera technology that makes our customers winners. Innovation requires equal parts of inspiration and hard work. We are fortunate to have a gifted and intensely customer-focused Altera team working around the world to create Altera's success.

Our customers are also key to the progress we made during this year of great change. I have learned from visiting these customers during this, my first full year at Altera, that their interest in programmable technology is expanding and they are pleased to see our ongoing technical leadership bring them more value. The insights we gained from them helped shape our products in countless ways.

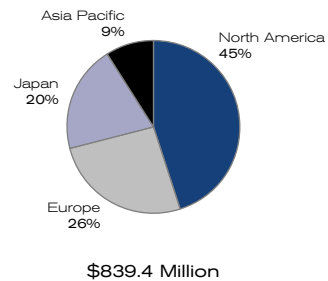
We also communicated frequently with our shareholders and are very grateful for the encouragement we have received during this particularly difficult year. We remain committed to keeping our focus on building value for our shareholders both today and the years ahead.

Thank you for your support.

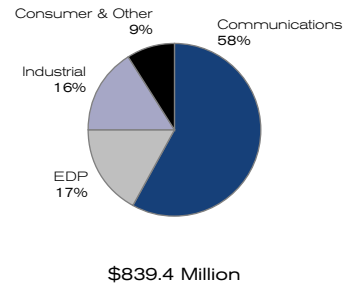


**John Daane**  
**President and Chief Executive Officer**

**2001 Revenue by Geographic Channel**



**2001 Revenue by Market Segment**



## Selected Consolidated Financial Data

### Five-Year Summary

Years ended December 31,

(In thousands, except per share amounts)

	2001	2000	1999	1998	1997
<b>Statements of Operations Data:</b>					
Net sales	\$ 839,376	\$1,376,815	\$ 836,623	\$ 654,342	\$ 631,114
Cost of sales	458,699	466,994	301,322	249,474	236,958
Gross margin	380,677	909,821	535,301	404,868	394,156
Research and development expenses	170,869	172,373	86,065	59,864	54,417
Selling, general, and administrative expenses	215,318	209,979	143,214	113,161	112,784
Acquired in-process research and development expense	—	6,305	—	—	—
Restructuring and other special charges	47,669	—	—	—	—
Income (loss) from operations	(53,179)	521,164	306,022	231,843	226,955
Gain on sale of WaferTech, LLC	—	178,105	—	—	—
Interest and other income, net	40,176	46,145	37,055	12,340	2,616
Income (loss) before income taxes, equity investment, and cumulative effect of change in accounting principle	(13,003)	745,414	343,077	244,183	229,571
Provision for income taxes	26,779	247,107	111,499	79,356	78,054
Equity in loss of WaferTech, LLC	—	1,400	7,584	10,440	—
Cumulative effect of change in accounting principle	—	—	—	—	18,064
Net income (loss)	\$ (39,782)	\$ 496,907	\$ 223,994	\$ 154,387	\$ 133,453
Net income (loss) per share:					
Basic	\$ (0.10)	\$ 1.25	\$ 0.57	\$ 0.41	\$ 0.38
Diluted	(0.10)	1.19	0.54	0.39	0.34
Shares used in computing income (loss) per share:					
Basic	386,097	396,849	396,158	373,972	354,100
Diluted	386,097	416,629	414,928	406,356	410,464
<b>Balance Sheet Data:</b>					
Working capital	\$ 882,421	\$1,013,155	\$ 785,359	\$ 587,923	\$ 430,371
Total assets	1,361,427	2,004,134	1,439,599	1,093,331	952,518
Long-term debt	—	—	—	—	230,000
Stockholders' equity	1,114,500	1,247,930	1,118,073	881,721	536,687
Book value per share	2.89	3.21	2.81	2.26	1.50

**SECURITIES AND EXCHANGE COMMISSION**  
**Washington, D.C. 20549**

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**Form 10-K**

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☒ (Mark One)  
ANNUAL REPORT PURSUANT TO SECTION 13 OR 15(d) OF THE  
SECURITIES EXCHANGE ACT OF 1934

**For the Fiscal Year Ended December 31, 2001**

**OR**

☐ TRANSITION REPORT PURSUANT TO SECTION 13 OR 15(d) OF THE  
SECURITIES EXCHANGE ACT OF 1934

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Commission File Number: **0-16617**

**ALTERA CORPORATION**

(Exact Name of Registrant as Specified in its Charter)

**Delaware**

(State or Other Jurisdiction of  
Incorporation or Organization)

**77-0016691**

(I.R.S. Employer  
Identification No.)

**101 Innovation Drive, San Jose, California 95134**

(Address of Principal Executive Offices) (Zip Code)

Registrant's Telephone Number, Including Area Code: **(408) 544-7000**

Securities registered pursuant to Section 12(b) of the Act:

**None**

Securities registered pursuant to Section 12(g) of the Act:

**Common Stock, \$0.001 par value per share**

(Title of Class)

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Indicate by check mark whether the registrant: (1) has filed all reports required to be filed by Section 13 or 15(d) of the Securities Exchange Act of 1934 during the preceding 12 months (or for such shorter period that the registrant was required to file such reports), and (2) has been subject to such filing requirements for the past 90 days. Yes ☒ No ☐

Indicate by check mark if disclosure of delinquent filers pursuant to Item 405 of Regulation S-K is not contained herein, and will not be contained, to the best of registrant's knowledge, in definitive proxy or information statements incorporated by reference in Part III of this Form 10-K or any amendment to this Form 10-K. ☐

The aggregate market value of the registrant's common stock held by non-affiliates of the registrant was approximately \$6,219,599,000 as of February 19, 2002, based upon the closing sale price on the Nasdaq National Market for that date. For purposes of this disclosure, shares of common stock held by persons who hold more than 5% of the outstanding shares of common stock and shares held by officers and directors of the registrant have been excluded because such persons may be deemed affiliates. This determination is not necessarily conclusive.

There were 385,843,466 shares of the registrant's common stock issued and outstanding as of February 19, 2002.

**DOCUMENTS INCORPORATED BY REFERENCE**

Item 6 of Part II incorporates information by reference from the Annual Report to Stockholders for the fiscal year ended December 31, 2001.

Items 10, 11, 12, and 13 of Part III incorporate information by reference from the Proxy Statement for the Annual Meeting of Stockholders to be held on April 30, 2002.

*Except for the historical information presented, the matters discussed in this Report include forward-looking statements, as further described under Item 7 and elsewhere in this Report. Forward-looking statements can be identified by the use of forward-looking words, such as “may,” “could,” “expect,” “believe,” “plan,” “anticipate,” “continue,” or other similar words.*

## **PART I**

### ***Item 1. Business.***

Altera Corporation designs, manufactures, and markets (1) high-performance, high-density programmable logic devices, or PLDs, (2) intellectual property cores, which are also known as megafunctions, and (3) associated development tools. Our PLDs, which consist of field-programmable gate arrays, or FPGAs, and complex programmable logic devices, or CPLDs, are semiconductor integrated circuits that our customers can program using our proprietary software, which operates on personal computers and engineering workstations. Intellectual property cores are pre-verified hardware description language, or HDL, design files for complex, yet commonly used system-level logic functions.

Founded in 1983 and reincorporated in Delaware in 1997, we were one of the first suppliers of complementary metal oxide semiconductor, or CMOS, PLDs and are currently a global leader in this market. Today, we offer a broad range of general-purpose PLDs that offer unique features as well as differing densities and performance specifications for implementing particular applications. Our products serve a wide range of markets, including telecommunication, data communication, electronic data processing, computer peripheral, and industrial applications. Some of our major products are more fully described below.

#### ***Overview of the Types of Integrated Circuits***

Three principal types of digital integrated circuits are used in most electronic systems: microprocessors, memory, and logic. Microprocessors are used for control and computing tasks; memory is used to store programming instructions and data; and logic is used to manage the interchange and manipulation of digital signals within a system. While system designers employ a relatively small number of standard architectures to meet their microprocessor and memory needs, they require a wide variety of logic circuits to differentiate their end products. In addition, competitive pressures force electronic systems manufacturers to reduce the size of their products and accelerate their products' introduction to market. At the same time, as new technologies evolve, customers require an even larger number of logic gates on a single integrated circuit for improved functionality, performance, reliability, and cost.

We believe that these competitive pressures are driving electronic systems manufacturers more towards system-on-a-programmable-chip, or SOPC, solutions. An SOPC solution includes an integrated, high-density PLD containing three or more of the following: logic, memory, high-speed I/O, and a processor. With SOPC solutions, system designers require less, if any, separate microprocessor or memory chips, thereby allowing them to reduce the size of their system designs.

#### ***Overview of the Logic Market***

According to Dataquest, the CMOS logic market consists of the following segments:

- Semi-custom or application-specific integrated circuits, or ASICs
- Standard logic
- Full custom devices
- Other forms of logic integrated circuits, including chipsets

The ASIC segment of the CMOS logic market is comprised of programmable logic, gate arrays, and cell-based integrated circuits, also referred to as standard cells. In a broad sense, all of these devices are indirectly competitive as they generally may be used in the same types of applications in electronic products. However, differences in cost, performance, density, flexibility, ease-of-use, and time-to-market dictate the extent to which they may be directly competitive for particular applications.

Programmable logic's primary advantage over gate arrays and standard cells is that it allows for quicker design cycles, meeting customers' needs for quick time-to-market. Programmable logic allows customers to experiment and revise their designs in a relatively short amount of time and with minimum cost. In most instances, this is quicker and easier than achieving a design through mask-programmed, fixed-logic gate arrays, as is required for gate arrays and standard cells. This advantage is amplified by the ability to have working chips at the time the design is finalized.

Another advantage of programmable logic over gate arrays and standard cells is that, particularly for low-volume applications, PLDs reduce development costs by lowering the per unit cost of producing customized components. PLDs inherently consume more silicon than other non-PLD ASIC devices because of the general application and on-chip programming capabilities of PLDs. However, depending on the complexity of the design and total unit requirements, this higher per unit cost of PLDs is, in many cases, more than offset by the high fixed costs of layout and mask-making required to produce a custom integrated circuit. Further, because unprogrammed PLDs are standard devices, we and our distributors—not our customers—hold stocks of inventory, thereby enhancing the cost advantage of PLDs for our customers. By holding large inventory stock, however, we also subject ourselves to the risk of inventory obsolescence, which occurred last year. We have recently changed our inventory carrying policy to more of a build-to-order basis, which we believe may reduce the risk of inventory obsolescence without sacrificing customer requirements.

### ***Strategy and Competition***

The primary attributes of ASICs are high density, high speed, and low production costs in high volumes. We compete with ASIC manufacturers on the basis of lower design costs, shorter development schedules, and reduced inventory risk and field upgradability. In general, high-volume, non-PLD ASIC devices cost less than PLDs; however, as PLDs have increased in density and performance and decreased in costs, they have become more directly competitive with other ASICs, especially gate arrays. Our strategy is to compete with other companies in the ASIC segment of the CMOS logic market by providing a total solution for our customers' logic needs. To accomplish this goal, we offer our customers:

- PLDs, including SOPC solutions, with the speed, density, functionality, and package types to meet their specific needs
- HardCopy™ devices that enable our customers to move from a PLD to a low-cost, custom implementation of their designs
- State-of-the-art development tools that are easy to use and compatible with other industry-standard electronic design automation, or EDA, tools
- Optimized system-level megafunctions to speed their design process
- A complete customer support system

We have been able to introduce new product families that, as compared to their predecessors, provide greater functionality at a lower price for any given density because high-volume manufacturing and emerging process technologies have resulted in cost decreases. We believe that in certain circumstances these new product families achieve the integration, density, performance, and cost advantages of other ASIC solutions. We also believe that our competitiveness within the ASIC segment in these areas, along with the inherent advantages of programmable logic discussed above, will enable us to compete for designs traditionally served by other ASIC devices.

In addition to competition in the broader ASIC market, we experience significant direct competition from other companies, including Xilinx, Inc. and Lattice Semiconductor Corporation, that are in the programmable logic sub-segment. We expect that as the dollar volume of the programmable logic sub-segment grows, the attractiveness of this sub-segment to larger, more powerful competitors will continue to increase.

The principal factors of competition in the programmable logic sub-segment of the ASIC market include:

- The capability of software development tools and system-level functional programming blocks
- Product performance and features
- Quality and reliability
- Pricing
- Technical service and customer support
- Technical innovation

We believe that we compete favorably with respect to these factors and that our proprietary device architecture and our installed base of development systems with proprietary software may provide some competitive advantage. However, as is true of the semiconductor industry as a whole, the ASIC segment and the PLD sub-segment are intensely competitive and are characterized by rapid technological change, rapid rates of product obsolescence, and price erosion. All of these factors may influence our future operating results. For a discussion of risk factors associated with our strategy and competition, see Item 7—Future Results; Risk Factors—“*Our financial results depend on our ability to compete successfully in the highly competitive semiconductor industry*” and “*Our future success depends on our ability to define, develop, and sell new products.*”

## **Products**

Our products consist primarily of devices, intellectual property cores, and proprietary development tools. Altogether, these products form a unique and comprehensive solution for the implementation of SOPC applications. A brief overview of these products is provided below.

## **Devices**

Our devices fall into the following three categories: (1) FPGAs; (2) general-purpose CPLDs; and (3) low-cost, masked devices. These devices span multiple architectures and device families, with a total of more than 1,000 product options. Each device family offers unique functional benefits and differing density and performance specifications for implementing particular applications.

### *FPGAs*

Our FPGAs consist of general-purpose FPGAs and embedded intellectual property-based, or IP-based, system products.

#### General-Purpose FPGAs

Our general-purpose FPGA products, consisting of our Stratix™, APEX™ II, APEX, FLEX®, and ACEX® product families, are built using the most advanced CMOS static random access memory, or SRAM, process technology and address a broad range of datapath applications from sub-system logic integration to SOPC applications. The basic logic building block in a general-purpose FPGA is the logic element, which is comprised of a look-up table and a storage element known as a flipflop. Therefore, the total number of logic elements in a given device is often used to gauge relative logic density among FPGAs. In addition, the amount of embedded RAM within general-purpose FPGAs is also identified in determining relative memory density. Including our newly announced Stratix device family, our general-purpose FPGAs provide up to 114,140 logic elements and up to 10 megabits of RAM in a single device, while offering industry-leading core and I/O performance levels.

Some of our major general-purpose FPGAs are more fully described below:

**STRATIX:** We publicly announced our Stratix architecture in February 2002 and plan to ship our first device in this family during the summer of 2002. Based on an industry-leading 1.5-V, 0.13-micron process, the Stratix device family provides high-bandwidth, SOPC integration for the communication, networking, high-end consumer, data storage, and industrial markets. This highly innovative architecture, which enables block-based design methodology, can range in density from 10,570 to 114,140 logic elements, includes up to 10 megabits of embedded RAM, and contains all-layer-copper interconnect technology, which results in greater performance compared to traditional aluminum/tungsten interconnect. Our Stratix devices also contain TriMatrix™ memory, which not only offers high memory density, but also maximum memory bandwidth by incorporating three memory block sizes of 512 bits, 4 kilobits, and 512 kilobits within each Stratix device. In addition, the embedded digital signal processing, or DSP, blocks provide ultra-fast performance for applications such as encryption and filtering in wireless communications, image processing in digital entertainment, and quality of service algorithms in data communications. Stratix devices also incorporate a variety of single-ended and differential I/O standards, with up to 116 high-speed differential I/O

channels with up to 80 channels optimized for 840 megabits per second per channel. Devices in this family provide support for various high-speed networking and communication bus standards.

*APEX II:* Utilizing a second-generation APEX architecture, the 1.8-V APEX II device family is designed to address the increasing performance and bandwidth requirements of communication applications. These look-up table devices are based on 0.13-micron and 0.15-micron processes and include all-layer-copper interconnect technology. They range in density from 16,640 to 67,200 logic elements and include over 1.0 megabit of embedded RAM. Our APEX II devices support low-voltage differential signaling, or LVDS, low-voltage positive-referenced emitter coupled logic, or LVPECL, and I/O speeds of up to 1.0 gigabits per second per channel.

*APEX 20K, APEX 20KE, and APEX 20KC:* Based on the APEX architecture, the 2.5-V APEX 20K, 1.8-V APEX 20KE, and 1.8-V APEX 20KC device families provide design flexibility and efficiency for high-performance SOPC applications. Our APEX 20KC family was also the first PLD family to utilize copper for all layers of metal interconnect. Devices in these families range in density from 1,200 to 51,840 logic elements, include up to 432 kilobits of embedded RAM, and were the first FPGAs to utilize an embedded system block, or ESB, to embed content addressable memory, or CAM, used in packet switching. Additionally, these devices contain enhanced phase-locked loops, or PLLs, for high-speed clock management, and LVDS for I/O speeds of up to 840 megabits per second per channel used in high-bandwidth communications and backplane applications.

*FLEX 10K, FLEX 10KA, and FLEX 10KE:* Based on the FLEX 10K architecture, which was the first PLD architecture to provide on-chip embedded memory, the 5.0-V FLEX 10K, 3.3-V FLEX 10KA, and 2.5-V FLEX 10KE device families offer embedded array blocks, or EABs, to provide a combination of logic and embedded RAM on a single-chip architecture for high-speed, high-bandwidth applications. These families range in density from 576 to 12,160 logic elements, include up to 96 kilobits of embedded RAM, and incorporate dual-port RAM.

*ACEX 1K:* Our ACEX 1K device family, which combines logic elements and EABs, offers complete system-level integration on a single device for cost-sensitive, volume-driven applications such as cable modems, xDSL modems, low-cost switches, and routers. Devices in this family range in density from 576 to 4,992 logic elements, include up to 48 kilobits of embedded RAM, and operate at a 2.5-V supply voltage.

#### Embedded IP-Based System Products

As a complement to our general-purpose FPGAs, our embedded IP-based system products combine a general-purpose FPGA architecture with embedded IP, or hard cores. Together, these two elements comprise a fully integrated and flexible, customizable solution for use in targeted applications. Our embedded IP-based system products consist of our Excalibur™ devices, which are targeted for applications requiring high-performance embedded microprocessors, and our Mercury™ devices, which are suited for applications that need embedded high-speed serial I/O, also known as a transceiver.

Our embedded IP-based system products are more fully described below:

*EXCALIBUR EMBEDDED PROCESSOR SOLUTIONS:* The Excalibur solutions combine logic, memory, and an embedded processor core, which together allow engineers to integrate an entire system on a single PLD for a wide range of applications, from 3G base stations, embedded routers, microcontrollers, and network processors to industrial control and factory automation. The Excalibur solutions consist of two embedded processor architectures: our Nios™ soft core embedded processor solution and the ARM®-based embedded processor solution. Our Nios soft core embedded processor was the industry's first soft core processor designed specifically for programmable logic. The Nios soft core utilizes a reduced instruction set computing, or RISC, architecture and is a cost-competitive and flexible alternative to discrete microcontroller solutions. The Nios soft core can be efficiently implemented in all of our general-purpose FPGA devices as well as in our IP-based system products. The ARM-based embedded processor PLD family uses technology licensed from ARM Limited and consists of multiple devices that each contains an ARM-based RISC processor core. These ARM-based Excalibur devices provide our customers with enhanced integration and royalty-free technology access for applications requiring the capability and complexity of an ARM processor while also needing the flexibility and customization of a general-purpose FPGA.

*MERCURY:* Our Mercury devices, which are programmable application-specific standard products, or ASSPs, address a wide range of serial backplane, chip-to-chip, and line-side applications. Providing speeds of up to 1.25 gigabits per second per

channel, these devices integrate a high-speed clock data recovery-enabled transceiver with a performance-optimized programmable logic core. The programmable logic core's performance is enabled using a prioritized interconnect structure, dedicated multiplier circuitry, and quad-port ESBs on a 1.8-V all-layer-copper process. Devices in this family range in density from 4,800 to 14,400 logic elements and include up to 112 kilobits of embedded RAM.

### *CPLDs*

Our general-purpose CPLD products, consisting of our MAX<sup>®</sup> and Classic<sup>™</sup> product families, are built using CMOS floating-gate process technology and address a wide range of high-speed glue logic applications. Glue logic is basic logic that enables the interaction of multiple subsystem components. The basic logic building block in a general-purpose CPLD is the macrocell. Therefore, the total number of macrocells within CPLDs is often used to gauge relative logic density. Another critical metric used in gauging CPLD performance is the total propagation delay, or  $t_{PD}$ , from an input pin to an output pin. Our MAX CPLDs provide over 500 macrocells in a single device with  $t_{PD}$  specifications as fast as 3.5 nanoseconds.

Some of our major general-purpose CPLDs are more fully described below:

*MAX 7000, MAX 7000S, MAX 7000A, and MAX 7000B:* Based on the widely popular MAX 7000 architecture, the 5.0-V MAX 7000, 5.0-V MAX 7000S, 3.3-V MAX 7000A, and 2.5-V MAX 7000B device families are among the most widely used programmable logic families in the industry. These device families provide high-density, high-speed, I/O-intensive programmable logic solutions for a broad range of glue logic applications, including state machines, control functions, and address decoding. Devices in these families range in density from 32 to 512 macrocells and provide  $t_{PD}$  values as fast as 3.5 nanoseconds. Features common to all current MAX 7000 devices include: (1) in-system programmability, or ISP, which allows devices to be programmed after they are soldered onto the printed circuit board, thereby minimizing the possibility of lead damage or electrostatic discharge exposure when reprogrammed, (2) the industry-standard Joint Test Action Group boundary-scan test, or JTAG BST, circuitry, which permits efficient board testing, (3) global clocking, (4) fast input registers, and (5) programmable slew-rate control.

*MAX 3000A:* The 3.3-V MAX 3000A devices, which range in density from 32 to 256 macrocells, target high-volume, low-cost glue logic applications. These devices support ISP and JTAG BST circuitry.

### *Masked Devices*

*HARDCOPY:* For our highest-density FPGA and embedded IP-based system products, our HardCopy devices combine proprietary silicon design and an automated migration process to offer our customers a seamless migration path to a mask-programmed implementation of their designs for low-cost and high-volume applications. As a result, HardCopy devices extend the flexibility, power, and time-to-market advantages of high-density PLDs to high-volume, more cost-sensitive applications traditionally covered by ASICs. We offer HardCopy devices for the Stratix, APEX II, APEX, and Excalibur products. These HardCopy devices offer up to a 70% die size reduction, resulting in a lower cost for customers seeking a high-volume production solution in our highest density devices.

## **Intellectual Property Cores**

Intellectual property cores are pre-verified HDL design files for complex, yet commonly used system-level logic functions. With intellectual property cores, system designers can focus more time and energy on improving and differentiating the unique aspects of the system design, rather than spending time designing common off-the-shelf functions from the ground up. Our intellectual property cores consist of MegaCore<sup>®</sup> functions, which we create internally, and Altera Megafunction Partners Program, or AMPP<sup>SM</sup>, cores, which are created by third parties. Today, we offer a broad range of intellectual property cores for various applications, including interface, memory controller, signal processing, telecommunication, data communication, microprocessor, and peripheral intellectual property cores.

## **Development Tools**

Our proprietary development tools, consisting of the Quartus<sup>®</sup> II and MAX+PLUS<sup>®</sup> II software, enable our customers to design for and program our PLDs. In particular, we believe that our Quartus II development software, a new version of which was released in February 2002, delivers improved designer productivity and supports system-level designs and integration with

third-party tools. Our Quartus II and MAX+PLUS II software development tools run under the Microsoft Windows and UNIX (including Solaris, HP-UX, and Linux) operating environments. Our development tools also provide interfaces to many industry-standard EDA tools, including those offered by Mentor Graphics Corporation, Synplicity, Inc., and Synopsys, Inc.

### ***Research and Development***

Our research and development activities have focused primarily on PLDs and on the associated development software and hardware. We have developed these related products in parallel to provide software support to customers upon device introduction. As a result of our research and development efforts, we have introduced during the past three years a number of new families, such as the Stratix, APEX II, APEX 20KC, Mercury, and HardCopy device families, as well as the Excalibur embedded processor solutions. We have also redesigned a number of our products to accommodate new wafer fabrication processes. In addition, we plan to release major versions of our proprietary software at least twice a year.

Our research and development expenditures were \$170.9 million in 2001, \$178.7 million in 2000, and \$86.1 million in 1999. Excluding a \$6.3 million one-time charge for acquired in-process research and development, our research and development expenditures in 2000 were \$172.4 million. We have not capitalized research and development or software costs to date. We intend to continue to spend substantial amounts on research and development in order to continue to develop new products and achieve market acceptance for such products, particularly in light of the industry pattern of short product life cycles and increasing competition within the CMOS logic market.

### ***Patents, Trademarks, and Licenses***

We generally rely on intellectual property law, including patent, copyright, trademark, and trade secret laws, to establish and maintain our proprietary rights in products and technology. As of December 31, 2001, we held a total of 622 patents relating to various aspects of our products and technology and have a number of patent applications currently pending. Also, we have used, registered, and applied to register certain trademarks and service marks to distinguish our products, technologies, and services from those of our competitors in the United States and foreign countries. In addition, we file registrations in the United States under the Semiconductor Chip Protection Act to protect our chip designs. Finally, we have entered into technology licensing agreements that give us rights to design, manufacture, and package products using certain intellectual property owned by others. In July 2001, we entered into a settlement agreement with Xilinx under which we settled all pending litigation between Altera and Xilinx. As part of the settlement agreement with Xilinx, Altera and Xilinx entered into a royalty-free patent cross license agreement, including a prohibition of further patent litigation between the two companies for the next five years. In connection with the settlement agreement, we paid Xilinx a one-time payment of \$20 million. Similarly, in July 2001 we entered into a settlement agreement with Lattice under which we settled all pending patent litigation between Altera and Lattice. As part of the settlement agreement with Lattice, Altera and Lattice entered into a royalty-free patent cross license agreement, including a multi-year prohibition of further patent litigation between the two companies. No payments were made by Altera or Lattice as part of the settlement.

When necessary, we seek to enforce our intellectual property rights. Although we believe that protection afforded by our intellectual property rights has value, the rapidly changing technology in the semiconductor industry makes our future success dependent primarily on the innovative skills, technological expertise, and management abilities of our employees rather than on our patent, trademark, or other proprietary rights. For a discussion of risk factors associated with our patents, trademarks, and licenses, see Item 3, Item 7—Future Results; Risk Factors — “*We may be unable to adequately protect our intellectual property rights and may face significant future litigation expenses,*” and Note 13 to our consolidated financial statements.

### ***Marketing and Sales***

We market our products in the United States, Canada, Europe, Japan, and Asia Pacific through a network of distributors and direct sales personnel. In the United States and Canada, we also rely on a network of independent sales representatives. From time to time, we may add or delete independent sales representatives or distributors from our selling organization as we deem appropriate to the level of business.

Throughout the United States, we have domestic sales management offices in major metropolitan areas. Our direct sales personnel and independent sales representatives focus on major strategic accounts. Distributors generally focus selling activities

on the broad base of small- and medium-size customers while providing demand fulfillment services to our major strategic accounts. Our only distributor in the United States is Arrow Electronics, Inc., which is responsible for creating customer demand from its customer base, providing technical support and other value-added services, filling customers' orders, and stocking our products.

Our international business is supported by a network of distributors in major European countries, Japan, and various countries throughout Asia Pacific. In addition, we maintain international sales support offices in the metropolitan areas of Helsinki, Hong Kong, Hsinchu (Taiwan), London, Munich, Ottawa, Paris, Seoul, Shanghai, Stockholm, Stuttgart, Tokyo, and Turin (Italy).

Through 2001, all international sales were denominated in U.S. dollars. For the year ended December 31, 2001, worldwide sales through distributors accounted for over 97% of total sales, and Arrow was, and continues to be, our largest distributor. In 2001 and 2000, two distributors accounted for more than 10% of sales. In 2001, one distributor accounted for 54% of sales, and the other distributor accounted for 13% of sales. In 2000, one distributor accounted for 58% of sales, and the other distributor accounted for 11% of sales. In 1999, three distributors accounted for more than 10% of sales. These three distributors accounted for 34%, 19%, and 13% of sales. The percentage increases for our largest distributor in 2001 and 2000 compared to 1999 are attributable to the combination of Arrow and Wyle Electronics, our two largest distributors in 2000. No single end customer accounted for more than 10% of our sales in 2001, 2000, or 1999. International sales constituted 55% of sales in 2001, 43% of sales in 2000, and 44% of sales in 1999.

For a detailed description of our sales by geographic region, see Item 7 and Note 14 to our consolidated financial statements.

### ***Backlog***

Our backlog of orders on December 31, 2001 was approximately \$119.6 million compared to approximately \$510.8 million on December 31, 2000. The significant decrease in backlog is attributable to a decrease in sales, together with a decrease in advance orders made by our customers. Our backlog consists of original equipment manufacturer, or OEM, orders and distributor orders that are each requested for delivery within the next three months. Prior to January 1, 2001, our OEM backlog consisted of OEM orders that were requested for delivery within the next six months. This change in the determination of OEM backlog did not materially affect the change in backlog from 2000 to 2001. Also, during the third quarter of 2001, we revised our inventory model to shift more towards a build-to-order strategy. Under our previous strategy, we built up inventory with standard products to enable us to ship our devices within a short time after receipt of an order. We do not believe that our build-to-order strategy will adversely affect our relationships with our customers.

Historically, backlog has been a poor predictor of future customer demand. While our backlog can increase during periods of high demand and supply constraints in certain products, our orders are generally cancelable without significant penalty at the option of the purchaser, thereby decreasing backlog during periods of lower demand. In addition, distributor shipments are subject to price adjustments. Further, we defer recognition of revenue on shipments to distributors until the product is resold to the end customer. For all of these reasons, backlog as of any particular date should not be used as a reliable predictor of sales for any future period.

### ***Customer Support***

Customer support and service are important aspects of selling and marketing our products. We provide several levels of technical user support, including applications assistance, design services, and customer training. Also, our applications engineering staff publishes data sheets and application notes, conducts technical seminars, and provides design assistance via Internet and electronic links to the customer's design station. Finally, as a service to our customer, inventory is maintained by us and our distributors to meet our customers' short-term delivery needs of our products.

## ***Manufacturing***

### **Wafer Supply**

We do not directly manufacture our silicon wafers. Instead, our silicon wafers are produced using various semiconductor foundry wafer fabrication service providers. This relationship enables us to take advantage of these suppliers' high volume economies of scale, as well as direct and more timely access to advancing process technology. We presently have our primary wafer supply arrangements with two semiconductor vendors: Taiwan Semiconductor Manufacturing Company, or TSMC, and Sharp Corporation. We may negotiate additional foundry contracts and establish other sources of wafer supply for our products as such arrangements become economically useful or technically necessary. For a discussion of risk factors associated with our wafer supply arrangements, see Item 7—Future Results; Risk Factors—*“We depend on independent subcontractors, located primarily in Asia, for the supply and quality of our finished silicon wafers.”*

### **Testing and Assembly**

After wafer manufacturing is completed, each wafer is tested using a variety of test and handling equipment. Such wafer testing is accomplished at TSMC, Sharp, and our San Jose pilot line facility, which is used primarily for new product development. This testing is performed on equipment owned by us and consigned to the vendors.

Resulting wafers are then shipped to various Asian assembly suppliers, where good die are separated into individual chips that are then encapsulated in ceramic or plastic packages. As is the case with our wafer supply business, we employ a number of independent suppliers for assembly purposes. This enables us to take advantage of subcontractor high-volume manufacturing, related cost savings, speed, and supply flexibility. It also provides us with timely access to cost-effective advanced process and package technologies. We purchase almost all of our assembly services from Amkor Electronics in Korea and the Philippines, ASAT Limited in Hong Kong, ASE, Inc. in Malaysia and Taiwan, and Fujitsu Microelectronics, Inc. in Japan.

Following assembly, each of the packaged units receives final testing, marking, and inspection prior to shipment to customers. We obtain almost all of our final test and back-end operation services from Amkor, ASAT, and ASE. Final testing by these assembly suppliers is accomplished through the use of our proprietary test software and hardware, which is consigned to or owned by such suppliers and/or third-party commercial testers. These suppliers also handle shipment of the products to our customers or distributors.

For a discussion of risk factors associated with our testing and assembly arrangements, see Item 7—Future Results; Risk Factors—*“We depend on independent subcontractors, located primarily in Asia, for the testing and assembly of our semiconductor products.”*

### ***Executive Officers of the Registrant***

Our executive officers and their ages are as follows:

<b><u>Name</u></b>	<b><u>Age</u></b>	<b><u>Position</u></b>
John P. Daane .....	38	President and Chief Executive Officer
Denis M. Berlan .....	51	Executive Vice President and Chief Operating Officer
Erik R. Cleage .....	41	Senior Vice President, Marketing
John R. Fitzhenry .....	52	Vice President, Human Resources
Lance M. Lissner .....	52	Senior Vice President, Business Development
George A. Papa .....	53	Senior Vice President, Worldwide Sales
Jordan S. Plofsky .....	41	Senior Vice President, Vertical Markets and Embedded Processor Products
Nathan M. Sarkisian .....	43	Senior Vice President and Chief Financial Officer
Katherine E. Schuelke .....	39	Vice President, General Counsel and Secretary

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There are no family relationships among our executive officers or between any executive officer and any of our directors.

**John P. Daane** has served as our President and Chief Executive Officer since November 2000 and as one of our directors since December 2000. Prior to joining us, Mr. Daane spent 15 years at LSI Logic Corporation, a semiconductor manufacturer, most recently as Executive Vice President, Communications Products Group. Mr. Daane earned his bachelors degree from the University of California, Berkeley in 1986.

**Denis M. Berlan** joined us in December 1989 as Vice President, Product Engineering and was named Vice President, Operations and Product Engineering in October 1994. In January 1996, he was named Vice President, Operations. In January 1997, he was named Executive Vice President and Chief Operating Officer. He was previously employed by Advanced Micro Devices, Inc., or AMD, a semiconductor manufacturer, and by Lattice Semiconductor Corporation, a semiconductor manufacturer, in engineering management capacities. Mr. Berlan received his M.S.E.E. in 1972 and Ph.D. in 1977 from the University of Grenoble in France and an M.B.A. in 1987 from the University of Santa Clara.

**Erik R. Cleage** joined us as International Marketing Manager in February 1986. He became Director, Japan and Asia Pacific Sales in April 1989, was appointed Vice President, Marketing in August 1990 and Senior Vice President, Marketing in January 1999. Previously, he was employed by AMD and Fairchild Semiconductor Corporation, a semiconductor manufacturer, in various positions. Mr. Cleage earned his bachelors degree from Stanford University in 1981.

**John R. Fitzhenry** joined us in May 1995 as Vice President, Human Resources. From February 1983 to May 1995, he was employed by Apple Computer, Inc., a manufacturer of personal computers, in various human resource management positions. Mr. Fitzhenry earned his bachelors degree from the University of California, Santa Barbara in 1971 and his J.D. from the University of the Pacific, McGeorge School of Law in 1976.

**Lance M. Lissner** joined us in May 1998 as Vice President of Business Development and Investor Relations and was appointed Senior Vice President, Business Development in November 2000. Prior to that time, Mr. Lissner was a corporate officer of Measurex Corporation, a developer of computer-integrated measurement, control, and information systems, where he was employed since 1973 and held various positions in sales, marketing, engineering, and business development. Mr. Lissner earned his bachelors degree from Harvey Mudd College in 1972 and his masters degree from Stanford University in 1973.

**George A. Papa** joined us in February 2002 as Senior Vice President, Worldwide Sales. From February 2000 to February 2002, Mr. Papa served as Vice President of Worldwide Sales of the Communications Business Group of Marvell Semiconductor, Inc., a semiconductor company. From March 1997 to February 2000, he served as Vice President of Worldwide Sales for Level One Communications, Inc., a subsidiary of Intel Corporation, a semiconductor company. From February 1991 to March 1997,

Mr. Papa served as Vice President of North American Sales for Siemens Corporation, a diversified global technology company. Mr. Papa earned his bachelors degree from Northeastern University.

**Jordan S. Plofsky** joined us in February 2001 and was appointed Senior Vice President, Vertical Markets and Embedded Processor Products as of March 2001. Prior to joining us, Mr. Plofsky was employed by LSI Logic from October 1996 to February 2001, most recently as Executive Vice President, Enterprise Infrastructure Group from November 2000 to February 2001 and Vice President and General Manager, Networking Products Division from June 1998 to November 2000. Mr. Plofsky earned a bachelors degree from the University of Illinois, Urbana-Champaign in 1982.

**Nathan M. Sarkisian** joined us in June 1992 as Corporate Controller. He was appointed Vice President, Finance and Chief Financial Officer in August 1995 and Senior Vice President and Chief Financial Officer in March 1998. Prior to joining us, Mr. Sarkisian held various accounting and financial positions at Fairchild and at Schlumberger Limited, an oil field services company. Mr. Sarkisian earned a bachelors degree from Stanford University in 1981 and an M.B.A. from Harvard University in 1992.

**Katherine E. Schuelke** joined us in March 1996 as Corporate Attorney. She became Senior Corporate Attorney in July 1997 and Assistant General Counsel and Assistant Secretary in July 1999. In October 2001, she was appointed Vice President, General Counsel and Secretary. Prior to March 1996, Ms. Schuelke was an attorney at the law firm of Morrison & Foerster LLP for seven years. Ms. Schuelke earned a bachelors degree from the State University of New York at Buffalo in 1986 and a J.D. from New York University in 1989.

### ***Employees***

As of December 31, 2001, we had 1,987 regular employees, including 861 in research and development, 39 in product engineering, 159 in operations, 595 in sales and marketing, and 333 in general management, administration, and finance. Of these employees, 1,314 were located in the United States, and 673 were employed in 16 other countries. None of our employees is represented by a labor union. We have not experienced any work stoppages, and we believe that our employee relations are good.

### ***Item 2. Properties.***

Our headquarters facility is located in San Jose, California on approximately 25 acres of land, which we purchased in June 1995. The campus for the headquarters facility currently consists of four interconnected buildings totaling approximately 500,000 square feet and a multi-level garage totaling approximately 260,000 square feet. Design, limited manufacturing, research, marketing, and administrative activities are performed in this facility. We also have a 240,000 square foot design and test engineering facility in Penang, Malaysia. This facility is situated on land leased on a long-term basis from the Penang Development Corporation. Finally, we lease on a short-term basis office facilities for our domestic and international sales management offices, our European Technology Center in the United Kingdom, our Toronto Technology Center, and our Ottawa Technology Center. Rental expense under all operating leases amounted to \$5.9 million in 2001. We believe that our existing facilities and planned future expansions are adequate for our current and foreseeable future needs.

### ***Item 3. Legal Proceedings.***

*We are a party to lawsuits and have in the past and may in the future become a party to lawsuits involving various types of claims, including, but not limited to, unfair competition and intellectual property matters. Legal proceedings tend to be unpredictable and costly and may be affected by events outside of our control. We cannot assure you that litigation will not have an adverse effect on our financial position or results of operations.*

In November 1999, we sued Clear Logic Inc. in the United States District Court for the Northern District of California, San Jose Division, alleging that Clear Logic is unlawfully appropriating our registered mask work technology in violation of the federal mask work statute and that Clear Logic has unlawfully interfered with our relationships and contracts with our customers. The lawsuit seeks compensatory and punitive damages and an injunction to stop Clear Logic from unlawfully using our mask work

technology and from interfering with our customers. Clear Logic has answered the complaint by denying that it is infringing our mask work technology and denying that it has unlawfully interfered with our relationships and contracts with our customers. Clear Logic also filed a counterclaim against us for unfair competition under California law alleging that we have made false statements to our customers regarding Clear Logic. In October 2001, the District Court ruled on summary judgment motions filed by both parties. The Court denied Clear Logic's motion for summary judgment of our claim of tortious interference with our software license, ruling that "using the bitstream [from our MAX+PLUS II software] to program a Clear Logic device violates Altera's software license." Further, the Court granted our motion for summary judgment disposing of Clear Logic's counterclaim of unfair competition. On January 4, 2002, Clear Logic filed a petition for Chapter 11 bankruptcy; as a result, all proceedings in the lawsuit have been automatically stayed. We moved to have this stay lifted, and the bankruptcy court granted our motion effective May 31, 2002. Due to the nature of the litigation with Clear Logic and because the lawsuit is still in the pre-trial stage, our management cannot estimate the total expenses that we will incur prosecuting the lawsuit. Although we cannot make any assurances as to the results of this case, we intend to pursue our claims vigorously.

In June 2000, Cypress Semiconductor Corporation sued us in the Santa Clara County Superior Court in San Jose alleging tortious interference with existing contractual relations with Right Track CAD Inc., tortious interference with economic relations, misappropriation of trade secrets, and unfair competition. In July 2000, we filed an answer that we had acquired Right Track in May 2000 and assumed the contract between Right Track and Cypress. In April 2001, Cypress added a claim based on fraud. Due to the nature of the litigation with Cypress and because the lawsuit is still in the pre-trial stage, our management cannot estimate the total expenses, the possible loss, if any, or the range of loss that may ultimately be incurred in connection with the allegations. Our management cannot ensure that Cypress will not succeed in obtaining significant monetary damages. Although we cannot make any assurances as to the results of this case, we intend to defend ourselves vigorously.

***Item 4. Submission of Matters to a Vote of Security Holders.***

None.

## PART II

### ***Item 5. Market for Registrant's Common Equity and Related Stockholder Matters.***

Our common stock trades on The Nasdaq National Market under the symbol "ALTR." As of February 19, 2002, there were approximately 713 stockholders of record. However, the majority of our shares are held by brokers and other institutions on behalf of approximately 117,200 stockholders as of February 19, 2002.

The closing price of our common stock on February 19, 2002 was \$22.10 per share as reported by The Nasdaq National Market. The following table sets forth, for the periods indicated, the high and low closing sale prices for our common stock as reported by The Nasdaq National Market, adjusted to reflect the effect of the July 2000 two-for-one stock split:

	<u>2001</u>		<u>2000</u>	
	<u>High</u>	<u>Low</u>	<u>High</u>	<u>Low</u>
First Quarter .....	\$34.31	\$21.44	\$48.50	\$24.00
Second Quarter.....	30.30	19.69	57.31	36.28
Third Quarter.....	32.88	15.77	64.81	43.97
Fourth Quarter.....	26.98	15.38	51.06	23.94

Our policy has been to reinvest earnings to fund future growth. Accordingly, we have not paid any cash dividends on our common stock and do not anticipate paying cash dividends in the foreseeable future.

### ***Item 6. Selected Financial Data.***

The section entitled "Selected Consolidated Financial Data" in our 2001 Annual Report is incorporated herein by reference.

### ***Item 7. Management's Discussion and Analysis of Financial Condition and Results of Operations.***

*The following Management's Discussion and Analysis of Financial Condition and Results of Operation, as well as information contained in "Future Results; Risk Factors" below and elsewhere in this Report, contains "forward-looking statements" within the meaning of Section 27A of the Securities Act of 1933 and Section 21E of the Securities Exchange Act of 1934. Forward-looking statements are not guarantees of future performance and involve risks and uncertainties, and actual results may differ materially from those projected in the forward-looking statements as a result of various factors. Forward-looking statements are generally written in the future tense and/or are preceded by words such as "will," "may," "should," "could," "expect," "suggest," "believe," "anticipate," "intend," "plan," or other similar words. Forward-looking statements include statements regarding (1) our gross margins and factors that affect gross margins, such as the costs of raw materials and our ability to absorb manufacturing costs, (2) our ability to control and reduce operating expenses, (3) our research and development efforts, (4) the commercial success of our new products, (5) the source of our revenues, (6) the availability of funds and cash to finance operations, (7) our ability to hold our fixed income investments until maturity, (8) future economic conditions, and (9) the impact of new accounting pronouncements.*

*Our future results of operations and the forward-looking statements contained in this Report involve a number of risks and uncertainties, many of which are outside of our control. Some of these risks and uncertainties are described in proximity to forward-looking statements in this Report. Factors that could cause actual results to differ materially from projected results include, but are not limited to, risks associated with (1) our ability to achieve continued cost reductions and maintain gross margins, (2) our ability to continue to achieve die size reductions, (3) our ability to achieve and maintain appropriate inventory mix and levels and respond successfully to changes in product demand, (4) the ability of price reductions to increase demand and strengthen our market share over the long term, (5) successful development and timely introduction of new products through investment in research and development and application of new process technologies to old and new product lines, (6) market acceptance of our new products, (7) continued demand for our existing products, (8) our ability to improve existing products, (9) the expected market demand for silicon wafers and potential supply shortages, (10) the ability of our subcontractors to*

*manufacture, assemble, test, and ship products efficiently and on a timely basis, (11) general market conditions, and (12) the impact of future litigation.*

*Although we believe that the assumptions underlying the forward-looking statements contained in this Report are reasonable, any of the assumptions could be inaccurate, and therefore there can be no assurance that such statements included in this Report will be accurate. In light of the significant uncertainties inherent in the forward-looking statements included herein, the inclusion of such information should not be regarded as a representation by us or any other person that the results or conditions described in such statements or our objectives and plans will be achieved.*

## **Overview**

We design, manufacture, and market high-performance, high-density PLDs, intellectual property cores, and associated development tools. PLDs are semiconductor chips that may be programmed on-site using software tools that run on personal computers or engineering workstations. User benefits include ease of use, lower risk, and fast time-to-market. Our products serve a wide range of markets, including telecommunication, data communication, electronic data processing, computer peripheral, and industrial applications. We offer our products in three categories: (1) FPGAs, which consist of our Stratix, APEX II, APEX, FLEX, ACEX, Excalibur, and Mercury products; (2) general-purpose CPLDs, which consist of our MAX and Classic products; and (3) low-cost, masked devices, which consist of our HardCopy product.

We classify our products into the following categories. All prior year data have been restated to reflect the following compositions:

- New products include APEX 20KE, APEX 20KC, APEX II, MAX 7000B, ACEX 1K, Excalibur, Mercury, HardCopy, and Stratix families
- Mainstream products include MAX 7000A, MAX 3000A, FLEX 6000, FLEX 10KA, FLEX 10KE, and APEX 20K families
- Mature and other products include Classic, MAX 7000, MAX 7000S, MAX 9000, FLEX 8000, and FLEX 10K families, configuration and other devices, tools, and intellectual property

## **Critical Accounting Policies**

**USE OF ESTIMATES** | The preparation of financial statements in conformity with accounting principles generally accepted in the United States of America requires management to make estimates and assumptions that affect the reported amounts of assets and liabilities and disclosure of contingent assets and liabilities at the date of the financial statements and the reported amounts of revenues and expenses during the reporting period. Actual results could differ from those estimates, and material effects on our operating results and financial position may result.

**INVENTORIES** | Inventories are recorded at the lower of standard cost, which approximates actual cost on a first-in-first-out basis, or market value. We write down inventories to net realizable value based on forecasted demand and market conditions. Actual demand and market conditions may be different from those projected by our management. This could have a material effect on our operating results and financial position. In 2001, as a result of unfavorable economic conditions and diminished demand for semiconductor products, we experienced a sharp decline in sales and recorded inventory charges of \$154.5 million related primarily to excess inventories. These charges have been included in cost of sales in our consolidated statements of operations. We have modified our inventory model to reduce inventory carrying levels and minimize the risk of excess inventory charges in the future.

**VALUATION OF PROPERTY, EQUIPMENT, AND INTANGIBLE ASSETS** | We evaluate the recoverability of our property and equipment and intangible assets in accordance with Statement of Financial Accounting Standards No. 121, or SFAS No. 121, "Accounting for the Impairment of Long-Lived Assets and for Long-Lived Assets to be Disposed of." This standard requires recognition of impairment of long-lived assets in the event the carrying value of such assets exceeds the future undiscounted cash flows attributable to such assets. Impairment evaluations involve management estimates of asset useful lives and future cash flows. Actual useful lives and cash flows could be different from those estimated by our management. This could have a material effect on our operating results and financial position.

In 2001, we recorded a charge of \$13.3 million for the impairment of production and other equipment that has been abandoned or is being held for sale, as well as for the impairment of purchased intangible assets related to technology acquired in previous acquisitions but no longer being used, and the impairment of investments in development stage enterprises that are in financial difficulties. These charges were classified as operating expenses in our consolidated statements of operations.

On January 1, 2002, SFAS No. 144, "Accounting for the Impairment or Disposal of Long-Lived Assets" became effective. This standard supersedes SFAS No. 121 and requires that one accounting model be used for long-lived assets to be disposed of by sale, whether previously held and used or newly acquired. Our adoption did not have a material effect on our financial statements.

**CONCENTRATIONS OF CREDIT RISK** | Financial instruments that potentially subject us to concentrations of credit risk consist principally of cash, cash equivalents, short-term investments, and accounts receivable. We place our cash, cash equivalents, and short-term investments in a variety of financial instruments and, by policy, limit the amount of credit exposure through diversification and by restricting our investments to highly rated securities. Diversification involves the use of management judgments and estimates. Actual results could differ from those estimates, and material effects on our operating results and financial position may result.

We sell our products to distributors and OEMs throughout the world. We perform ongoing credit evaluations of our customers' financial condition and generally require collateral whenever deemed necessary. We are highly dependent on our largest distributor, Arrow, to sell our products in many locations across the world, particularly in North America where Arrow is our only distributor.

**REVENUE RECOGNITION** | We recognize revenue from product sales upon shipment to OEMs and end users provided that persuasive evidence of an arrangement exists, the price is fixed, title has transferred, collection of resulting receivables is reasonably assured, there are no customer acceptance requirements, and there are no remaining significant obligations. Reserves for sales returns and allowances are recorded at the time of shipment. Our sales to distributors are made under agreements allowing for returns or credits under certain circumstances. We defer recognition of revenue on sales to distributors until products are resold by the distributor to the end user.

**DEPENDENCE ON WAFER SUPPLIERS AND OTHER INDEPENDENT SUBCONTRACTORS** | We do not directly manufacture finished silicon wafers. Our strategy has been to purchase silicon wafers from independent wafer foundries. We also depend on these wafer foundries to improve process technologies in a timely manner and to enhance our product designs and cost structure. Although there is presently good availability in the silicon market, semiconductor foundry capacity can become limited quickly and without much notice. We cannot assure you that any future shortage in foundry manufacturing capacity will not result in production problems for us in the future.

We also depend on independent subcontractors, located primarily in Asia, for the testing and assembly of our semiconductor products. Any unfavorable economic conditions, political strife, prolonged work stoppages, natural or man-made disasters, or power shortages in these countries, or other factors, may adversely affect the ability of our independent subcontractors to manufacture, test, and assemble our products, and therefore may have a material adverse effect on our operating results, financial position, and cash flows.

### **Results of Operations**

**SALES** | Sales were \$839.4 million in 2001, \$1,376.8 million in 2000, and \$836.6 million in 1999. Sales declined 39.0% in 2001 from 2000 and increased 64.6% in 2000 from 1999. The decline in sales in 2001 compared to 2000 was primarily due to lower unit sales of our Mature and Mainstream products and lower average unit selling prices in all product categories. The

increase in sales in 2000 compared to 1999 was primarily due to higher unit sales in all product categories, which was partially offset by decreases in average unit selling prices.

Sales by Product Category for 2001, 2000, and 1999 were as follows:

(Amounts in thousands)	Years Ended December 31,					
	2001	%	2000	%	1999	%
New	\$ 110,783	13.2%	\$ 52,097	3.8%	\$ 78	0%
Mainstream	383,297	45.7%	656,121	47.6%	253,571	30.3%
Mature and other	345,296	41.1%	668,597	48.6%	582,974	69.7%
Total sales	\$ 839,376	100.0%	\$1,376,815	100.0%	\$ 836,623	100.0%

Sales of New products were \$110.8 million in 2001, 112.6% higher than 2000 sales of \$52.1 million. Sales of Mainstream products were \$383.3 million, 41.6% lower than 2000 sales of \$656.1 million. Sales of Mature and other products were \$345.3 million, 48.4% lower than 2000 sales of \$668.6 million.

Our New and Mainstream products have been developed and introduced to the marketplace over the last several years. These products have similar or improved features and comparable or higher densities than their predecessors. As a result of increased customer demand for PLDs with higher densities and enhanced performance, we experienced a shift in sales to our newer products from our more mature products. New products sales increased both as a percentage of total sales and in absolute dollars primarily due to strong design win momentum in our New products. Our management expects that sales for our New products will continue to increase in 2002.

Sales by Market Segment for 2001, 2000, and 1999 were as follows:

(Amounts in thousands)	Years Ended December 31,					
	2001	%	2000	%	1999	%
Communications	\$ 489,273	58.4%	\$ 924,774	67.2%	\$ 555,001	66.3%
Electronic Data Processing/Computer	142,903	17.1%	237,782	17.3%	132,129	15.8%
Industrial	135,693	16.1%	143,577	10.4%	95,303	11.4%
Consumer	24,274	2.8%	28,251	2.0%	24,683	3.0%
Other	47,233	5.6%	42,431	3.1%	29,507	3.5%
Total sales	\$ 839,376	100.0%	\$1,376,815	100.0%	\$ 836,623	100.0%

As a result of unfavorable economic conditions and reduced capital spending by communication service providers that purchase our customers' products, sales from the communications market segment decreased significantly in 2001. Despite this decrease, we continued to generate the majority of our sales from the communications market segment, driven primarily by the telecommunication and networking sectors. Our management believes that the communications market segment will continue to drive the largest percentage of sales.

Effective January 1, 2002, we adopted a new methodology for revenue classification by market segment. The new classification includes Communications, Electronic Data Processing/Computer, Industrial and Automotive, and Digital Consumer. The new methodology reflects reclassifications between segments and is consistent with industry analyst reports.

Sales by Geography for 2001, 2000, and 1999 were as follows:

(Amounts in thousands)	Years Ended December 31,					
	2001	%	2000	%	1999	%
North America	\$ 377,275	44.9%	\$ 786,758	57.1%	\$ 469,368	56.1%
Europe	217,262	25.9%	300,229	21.8%	160,027	19.1%
Japan	166,565	19.9%	206,958	15.1%	158,513	19.0%
Asia Pacific	78,274	9.3%	82,870	6.0%	48,715	5.8%
Total International	462,101	55.1%	590,057	42.9%	367,255	43.9%
Total sales	\$ 839,376	100.0%	\$1,376,815	100.0%	\$ 836,623	100.0%

North America sales declined 52.0% in 2001 from 2000. North America sales represented 44.9% of total sales in 2001 compared to 57.1% in 2000 and 56.1% in 1999. The decreases, both in absolute dollars and in percentage of total sales, were primarily a result of unfavorable economic conditions that began to affect us in November 2000. Beginning in November 2000, we saw an inventory correction in our North American business driven primarily by an accumulation of inventory both at our customers and their subcontract manufacturers. During 2001, we experienced further declines in North America sales as a result of deteriorating end-market demand experienced by our North American communications equipment customers.

International sales declined 21.7% in 2001 from 2000. International sales represented 55.1% of total sales in 2001 compared to 42.9% in 2000 and 43.9% in 1999. Unfavorable economic conditions spread to Europe and Japan beginning in the second quarter of 2001, resulting in a 27.6% decline in sales in Europe and a 19.5% decline in sales in Japan for 2001 compared to 2000.

The fourth quarter of 2001 appears to be the bottom of this economic downturn, as we see increasing order strength and improved customer backlog. Our management expects that quarterly revenues will be flat or increase modestly starting in early 2002, but we cannot assure you that this will occur. If unstable and unfavorable economic conditions persist or worsen, or if a wider economic slowdown occurs, our future operating results could be further adversely affected.

In 2000, North America sales grew 67.6% from 1999, while sales in Europe grew 87.6%, Japan grew 30.6%, and Asia Pacific grew 70.1%.

Major items in the statements of operations, expressed as a percentage of sales, were as follows:

	Years Ended December 31,		
	2001	2000	1999
Cost of sales	54.6%	33.9%	36.0%
Gross margin	45.4%	66.1%	64.0%
Total research and development expenses	20.4%	13.0%	10.3%
Selling, general, and administrative expenses	25.7%	15.2%	17.1%
Restructuring and other special charges	5.6%	-	-
Income (loss) from operations	(6.3%)	37.9%	36.6%
Gain on sale of WaferTech, LLC	-	12.9%	-
Interest and other income, net	4.8%	3.4%	4.4%
Provision for income taxes	3.2%	17.9%	13.3%
Net income (loss)	(4.7%)	36.1%	26.8%

**GROSS MARGIN** | Gross margin, as a percentage of sales, was 45.4% in 2001, 66.1% in 2000, and 64.0% in 1999. The significant decrease in gross margin for 2001 was primarily a result of inventory charges taken during 2001 totaling \$154.5 million. The inventory charges, which resulted from sharp declines in sales, related primarily to excess inventory provisioning for our APEX 20KE, FLEX 10KE, and MAX 7000A product families and assembly packaging materials. In anticipation of

continued strong demand and to improve availability of our APEX 20KE and FLEX 10KE product families, we ordered wafers that were delivered in the fourth quarter of 2000 and the first quarter of 2001. These wafers became excess to demand as a result of the sharp contraction in sales. Excluding the inventory charge, gross margin was 63.8% for 2001 compared to 66.1% for 2000. This decrease in gross margin was due to routine declines in selling prices coupled with fixed unit costs, owing to high inventory levels. Additionally, reduced factory activity has resulted in under-absorbed manufacturing overhead. In the fourth quarter of 2001, we also started to engage in opportunistic deals and sold valued inventory at low prices, which resulted in a negative impact on our margins. Irrespective of the result of these potential opportunistic deals, our management expects that gross margins will decline gradually through the first half of 2002, but will begin to increase in the second half of the year. Our management also expects that routine declines in selling prices will be at least partially offset by improved manufacturing overhead absorption as we ramp production for certain depleted finished goods, and by lower die costs resulting from improved yields and lower wafer prices.

**RESEARCH AND DEVELOPMENT EXPENSES** | Research and development expenses for the year ended December 31, 2001 were \$170.9 million, or 20.4% of sales, compared to \$178.7 million, or 13.0% of sales, in 2000 and \$86.1 million, or 10.3% of sales, in 1999. Historically, the level of research and development expenses as a percentage of sales has fluctuated in part due to the timing of the purchase of masks and wafers used in the development of new products. We expect that, in the long term, research and development expenses will increase in absolute dollars primarily due to our efforts to develop new products. Research and development expenses include expenditures for labor, masks, prototype wafers, the amortization of deferred stock-based compensation for employees engaged in research and development activities, and expenses for the development of process technology, new packages, and software to support new products and design environments.

Despite unfavorable economic conditions, we continued to invest in the development of new products in order to maintain our competitive position. Excluding the \$6.3 million one-time acquired in-process research and development charge taken in 2000, research and development expenses remained relatively flat in 2001 compared to 2000. Research and development expenses increased \$86.3 million, or 100.2%, in 2000 compared to 1999. The increase in absolute dollars was primarily a result of increased headcount, additional spending on masks, prototype wafers, package development, and the development of our Quartus II software and Excalibur embedded processor solutions. During 2000, we recorded deferred stock-based compensation of \$41.3 million for the acquisitions of DesignPRO Inc. and Right Track CAD Inc. which is being amortized to research and development expenses over a period of three to four years. Amortization of deferred stock-based compensation included in research and development expenses was \$13.8 million for the year ended December 31, 2001 and \$8.3 million for the year ended December 31, 2000.

We expect to continue to invest in the development of new products, especially in our Stratix, APEX II, HardCopy, Mercury, and APEX 20KC families, as well as in our Excalibur embedded processor solutions, Quartus II software, and other future products. Our management expects these new products to be successful in the marketplace; however, the commercial success of these products depends on market acceptance of the use of the devices in high-density designs. We cannot assure you that any of our new products will achieve market acceptance. Some of our major achievements in 2001 and early 2002 are summarized below:

- We introduced our Stratix device family, which we believe is the industry's largest and fastest PLD. Stratix devices have relatively smaller die sizes while achieving high levels of integration with more memory, logic elements, and DSP functionality. The new high-performance Stratix architecture, which enables block-based design methodology, allows for easy integration of complex functions into a single PLD.
- We began shipping our APEX II device family, a high-performance, high-density PLD family for SOPC applications. Our APEX II family incorporates enhancements to both the I/O and memory structures, allowing designers to incorporate high-level system functionality onto a single PLD. Our APEX II EP2A70, the latest device in the APEX II family, began shipping in December 2001. This device is the industry's first PLD to use a 0.13-micron all-copper interconnect system, which provides greater performance versus traditional aluminum/tungsten interconnect.
- We began shipping our HardCopy devices, which facilitate a seamless migration path from the largest PLDs to a hard, masked version, offering a low-cost alternative for customers desiring high volumes. HardCopy devices are offered to support high-density APEX 20KE, APEX 20KC, APEX II, Excalibur, and Stratix devices. We believe the combination of PLDs and HardCopy devices will deliver the benefits of fast time-to-market, flexibility, and lower costs that are important to customers in today's markets.

- We began shipping our ARM-based Excalibur embedded processor solutions, which provide designers a reduction in overall development cost and accelerated time-to-market compared to ASIC solutions.
- We announced an enhancement of our Nios soft core processor, which is one of our Excalibur embedded processor solutions and enables engineers to easily integrate peripherals and implement entire systems onto a single PLD.
- We began shipping our Mercury device family, which integrates the functionality of a high-speed transceiver ASSP with a high-performance PLD core engineered to support high bandwidth and rapid data transfer rates.
- We began shipping our APEX 20KC device family, which utilizes copper for all layers of metal interconnect. Copper interconnect boosts performance and is thus appealing in high-bandwidth, high-performance applications.
- We released our Quartus II development software, which we believe delivers improved designer productivity and supports system-level designs and integration with third-party tools. The latest version of Quartus II development software, which provides further improvement in design performance and reduces compile times, was available beginning in February 2002.

Despite the current unfavorable economic conditions, we will continue to focus our efforts on the development of new PLDs and hardware that utilize advanced semiconductor wafer fabrication processes, as well as related development software. We cannot assure you that we will accomplish our goals in the development and subsequent introduction of new products, that our new products will achieve market acceptance, that new manufacturing processes will be successful, or that our suppliers will provide us with the quality and quantity of wafers and materials we require. We also cannot assure you that our new product introductions will be timely relative to product introductions by our competitors, which is critical in achieving market success.

**SELLING, GENERAL, AND ADMINISTRATIVE EXPENSES** | Selling, general, and administrative expenses for the year ended December 31, 2001 were \$215.3 million, or 25.7% of sales, compared to \$210.0 million, or 15.2% of sales, in 2000 and \$143.2 million, or 17.1% of sales, in 1999. Selling, general, and administrative expenses increased \$5.3 million, or 2.5%, in 2001, and \$66.8 million, or 46.6%, in 2000.

Selling, general, and administrative expenses include salary expenses related to field sales, marketing and administrative personnel, commissions and incentive expenses, advertising and promotional expenditures, and legal expenses. Selling, general, and administrative expenses also include costs related to the direct sales force and field application engineers who work in sales offices worldwide to stimulate demand by assisting customers in the use and proper selection of our products. The customers then work with our distributors for order fulfillment and logistical requirements. In 2001, over 97% of our sales are made through distributors.

Despite the slight increase in selling, general, and administrative expenses in 2001 compared to 2000, the amount of spending has dropped steadily during the year. The selling, general, and administrative spending in the fourth quarter of 2001 decreased 22.8% from our peak spending in the first quarter. The decrease was primarily due to spending control measures, including the restructuring program implemented during 2001. This restructuring program includes, but is not limited to, a worldwide workforce reduction mainly in administrative functions, the spin-off of a design service center, Northwest Logic, Inc., and the consolidation of excess facilities. In addition, we settled our Xilinx and Lattice litigation. We expect that selling, general, and administrative expenses will continue to slightly decline in absolute dollars as a result of reduced litigation expenses stemming from the settlement of the Xilinx and Lattice litigation and other spending control measures.

The increase in selling, general, and administrative expenses in 2000 compared to 1999 was mainly driven by increased headcount for sales, marketing, and administration personnel, higher advertising and legal expenses, and higher commission and incentive expenses associated with increased sales.

**RESTRUCTURING AND OTHER SPECIAL CHARGES** | During 2001, we recorded restructuring and other special charges of \$47.7 million in connection with our plan to align our organization's cost structure with projected sales resulting from the unfavorable economic conditions and to reduce future operating expenses. This restructuring program includes a worldwide workforce reduction, the spin-off of Northwest Logic, the write-down of certain equipment and intangible assets, the

consolidation of excess facilities, and the termination of certain license agreements. In addition, we settled our patent litigation with Xilinx. These charges were classified as operating expenses in our consolidated statements of operations.

A summary of the restructuring and other special charges is as follows:

(In thousands)	Total Charges	Non-cash Charges	Cash Payments	Restructuring Liability as of December 31, 2001
Workforce reduction	\$ 3,834	\$ 83	\$ 2,900	\$ 851
Litigation settlement	20,000	-	20,000	-
Spin-off of Northwest Logic	6,697	6,338	200	159
Impairment of production and other equipment	8,158	8,158	-	-
Impairment of investments and intangible assets	5,157	5,157	-	-
Consolidation of excess facilities and other	3,823	575	2,031	1,217
Total	\$ 47,669	\$ 20,311	\$ 25,131	\$ 2,227

#### *Workforce Reduction*

We reduced our worldwide workforce by approximately 152 employees primarily in administrative functions located mainly in our headquarters facility in San Jose, California. The workforce reduction resulted in a \$3.8 million charge relating primarily to severance and fringe benefits. Additionally, we initiated cost reduction measures, which included a temporary reduction of executive officer pay by 10% and the cancellation of employee merit increases. We also reduced the number of temporary and contract workers and, starting in the first quarter of 2001, did not replace voluntary attrition except for key positions.

#### *Litigation Settlement*

In connection with the settlement of litigation with Xilinx, we entered into a royalty-free patent cross license agreement and agreed to make a one-time payment of \$20.0 million. Both companies also agreed to refrain from instituting further patent litigation between our two companies for the next five years.

#### *Spin-Off of Northwest Logic*

We completed the spin-off of Northwest Logic to two of its employees in December 2001. Northwest Logic was a design service center that we acquired in 2000. The spin-off resulted in the termination of 14 employees. We recorded a charge of \$6.7 million related primarily to stock-based compensation of \$4.3 million for the acceleration of unvested stock options of terminated employees, as well as severance, fringe benefits, and the write-off of certain tangible and intangible assets and liabilities relating to Northwest Logic.

#### *Impairment Loss on Equipment, Investments, and Intangible Assets*

We recorded a charge of \$8.2 million for the impairment of production and other equipment that has been abandoned or is being held for sale. Certain production equipment is now surplus to our requirements and marketed for sale. We reclassified \$1.4 million from property and equipment to other current assets in our consolidated balance sheet to reflect our intention to sell these assets within the next twelve months. The amount reclassified represents the estimated net realizable value of equipment that is being held for sale. We also recorded a \$5.2 million charge resulting from the impairment of purchased intangible assets related to technology acquired in previous acquisitions but no longer being used, as well as investments in development stage enterprises that are in financial difficulties.

#### *Consolidation of Excess Facilities and Other*

We recorded a charge of \$3.8 million resulting from the consolidation of excess facilities primarily related to lease terminations and non-cancelable lease costs, as well as other charges including the termination of certain license agreements.

We substantially completed the implementation of our restructuring program in 2001. Amounts related to the termination of agreements and non-cancelable leases will be paid over their respective terms through the third quarter of 2005. Cash expenditures relating to workforce reductions will be paid by the first half of 2003. The restructuring liability, totaling \$2.2 million as of December 31, 2001, is included in accrued liabilities in the consolidated balance sheet.

We expect that the reductions in legal expenses, depreciation, amortization, and labor expense resulting from the restructuring program and voluntary attrition will reduce our operating expenses by more than \$8.0 million on a quarterly basis. These savings started to phase-in during the second half of 2001.

**IN-PROCESS RESEARCH AND DEVELOPMENT** | During 2000, we recorded a non-recurring charge of \$6.3 million to in-process research and development related to the acquisition of DesignPRO and Right Track. We determined this non-recurring charge using valuation techniques generally used by appraisers in the high-technology industry. We immediately expensed this non-recurring charge in the period of acquisition because technological feasibility had not been established and no alternative use had been identified. As of December 31, 2001, we believe that the projections used in the valuations with respect to each acquisition are still materially valid; however, there can be no assurance that the projected results will be achieved.

**INCOME (LOSS) FROM OPERATIONS** | Loss from operations was \$53.2 million, or 6.3% of sales, for the year ended December 31, 2001 compared to operating income of \$521.2 million, or 37.9% of sales, in 2000 and operating income of \$306.0 million, or 36.6% of sales, in 1999. The decrease in operating income in 2001 was primarily due to a decline in sales as well as the inventory, restructuring, and other special charges taken in 2001. The increase in operating income in 2000, as a percentage of sales, was primarily due to improvements in gross margin and a decrease in selling, general, and administrative expenses, partially offset by increased research and development expenses.

**INTEREST AND OTHER INCOME, NET** | Interest and other income was \$40.2 million, or 4.8% of sales, for the year ended December 31, 2001 compared to \$46.1 million, or 3.4% of sales, in 2000 and \$37.1 million, or 4.4% of sales, in 1999. The decline in absolute dollars in 2001 compared to 2000 was primarily due to lower interest rates and lower investment balances. Interest and other income consists mainly of interest income generated from investments in high-quality fixed income securities.

For the year ended December 31, 1999, interest and other income included a one-time pre-tax gain of \$10.3 million from the sale of the MAX 5000 family and our equity interest in Cypress Semiconductor (Texas), Inc. Excluding the one-time gain, interest and other income was \$26.8 million, or 3.2% of sales. Excluding the one-time gain, the increase from 1999 to 2000, in both absolute dollars and as a percentage of sales, was primarily due to an increase in interest income related to higher investment balances and higher interest rates.

**PROVISION FOR INCOME TAXES** | Our effective tax rates were (205.9%) for 2001, 33.2% for 2000, and 32.5% for 1999. Excluding the inventory, restructuring, and other special charges taken in 2001 and a one-time gain on the sale of WaferTech, LLC in 2000, our effective tax rates were 30.0% for 2001, 31.0% for 2000, and 32.5% for 1999. The reduction of the effective tax rate, as measured on this basis, over the three year period primarily resulted from a change in the geographic mix of income.

**EQUITY INVESTMENT** | In June 1996, we formed WaferTech, LLC, a joint venture company, with TSMC and several other partners to build and operate a wafer manufacturing plant in Camas, Washington. WaferTech began production of silicon wafers in October 1998 and achieved volume production in 1999. On December 27, 2000, we sold our 23% ownership interest in WaferTech to a subsidiary of TSMC for \$350.4 million in cash. The one-time pre-tax gain on the sale of WaferTech was \$178.1 million. Although we sold our equity interest in WaferTech in December 2000, we expect to continue utilizing WaferTech as one of our suppliers of silicon wafers. Through December 27, 2000, we accounted for our investment under the equity method based on our ability to exercise significant influence over WaferTech's operating and financial policies. Our equity in the loss of WaferTech was \$1.4 million for 2000 and \$7.6 million for 1999.

### **Financial Condition, Liquidity, and Capital Resources**

**YEAR 2001** | We ended 2001 with \$805.7 million of cash, cash equivalents, and short-term investments available to finance our operating activities and future growth. Since our inception, we have used a combination of equity and debt financing and

cash generated from operations to support our operating activities and capital expenditures, make acquisitions and investments, and repurchase our common stock under our stock repurchase program.

In 2001, our primary cash usage included \$183.2 million for the repurchase our common stock, compared to \$555.5 million used in 2000, and \$87.1 million used in 1999. We also used \$65.8 million for purchases of capital equipment in 2001, compared to \$87.5 million in 2000, and \$29.8 million in 1999. Our management believes that capital expenditures will be significantly lower in 2002 compared to 2001. We also lease certain of our sales facilities under non-cancelable lease agreements expiring at various times through 2009. Rental expense amounted to \$5.9 million in 2001. We anticipate that our lease payments in 2002 will approximate 2001. We believe the available sources of funds including cash, cash equivalents, and short-term investments, and cash we expect to generate from operations will be adequate to finance our activities for at least the next year.

Future minimum lease payments are as follows:

Years ending December 31,	(In thousands)
2002	\$ 6,041
2003	5,013
2004	4,289
2005	3,875
2006	2,186
Thereafter	4,304
Total	<u>\$ 25,708</u>

Cash and cash equivalents decreased \$351.3 million, or 70.8%, to \$145.0 million at December 31, 2001 from \$496.4 million at December 31, 2000. The decrease resulted from \$118.3 million used for operating activities, \$84.1 million used for investing activities, and \$148.9 million used for financing activities. Our negative cash flow from operations was primarily attributed to our net loss, decreases in deferred income on sales to distributors, accounts payable, accrued compensation, and income taxes payable, and an increase in other current assets. These items were partially offset by depreciation and amortization, amortization of deferred stock-based compensation, and decreases in inventories, accounts receivable, and deferred income taxes.

Accounts receivable decreased \$135.0 million, or 79.9%, to \$33.9 million at December 31, 2001 from \$168.9 million at December 31, 2000. Days sales outstanding in receivables decreased to 19 days at December 31, 2001 from 42 days at December 31, 2000. The decrease in accounts receivable and days sales outstanding was primarily due to a decrease in billings to distributors, which resulted from a decrease in end customer sales as well as a reduction of distributor inventory to align with lower sales.

Inventories decreased \$196.0 million, or 71.6%, to \$77.6 million at December 31, 2001 from \$273.6 million at December 31, 2000. The decrease was mainly due to inventory charges of \$154.5 million taken in 2001. In anticipation of continued strong demand and to improve availability of our APEX 20KE and FLEX 10KE product families, we ordered wafers that were delivered in the fourth quarter of 2000 and the first quarter of 2001. These wafers became excess to demand as a result of the sharp contraction in sales. Inventory months supply on hand was 3.6 at December 31, 2001 and 6.6 at December 31, 2000. Our management has modified our inventory model to reduce inventory carrying levels to minimize the risk of excess inventory charges in the future.

Cash payments in connection with the restructuring program were \$25.1 million since the inception of the program. We expect that the reductions in legal expenses, depreciation, amortization, and labor expense resulting from the restructuring program and voluntary attrition will reduce our operating expenses by more than \$8.0 million on a quarterly basis. These savings started to phase-in during the second half of 2001.

During 2001, cash used for investing activities of \$84.1 million consisted of purchases of capital equipment, short-term investments as well as long-term investments. Cash used for financing activities of \$148.9 million resulted from the repurchase of 7.2 million shares of our common stock, which was partially offset by net proceeds from the issuance of 4.3 million shares of our common stock to employees through various option plans and our employee stock purchase plan.

**YEAR 2000** | We ended 2000 with \$1,133.6 million of cash, cash equivalents, and short-term investments. Cash and cash equivalents increased \$332.1 million, or 202.1%, to \$496.4 million at December 31, 2000 from \$164.3 million at December 31, 1999. The increase resulted from \$550.4 million provided by operating activities, \$290.3 million provided by investing activities, partially offset by \$508.6 million used for financing activities. Our positive cash flow from operations was primarily attributed to our net income, increases in income taxes payable, deferred income on sales to distributors, accounts payable and accrued liabilities, a decrease in other current assets, the one-time write-off of acquired in-process research and development, depreciation, and amortization as well as amortization of deferred stock-based compensation. These items were partially offset by increases in inventories, deferred income taxes, and accounts receivable. Cash from operating activities was also offset by the gain of \$178.1 million on the sale of WaferTech.

Cash generated from investing activities of \$290.3 million consisted of cash proceeds of \$350.4 million from the sale of our equity interest in WaferTech and net sales of short-term investments of \$43.0 million. These items were partially offset by cash payments for the acquisitions of DesignPRO and Right Track for \$11.5 million and the purchase of certain long-term investments. In addition, we invested \$87.5 million primarily in land, manufacturing and data processing equipment and software, and building improvements in our headquarters and Penang facilities.

Cash used for financing activities of \$508.6 million resulted from the repurchase of 17.1 million shares of our common stock, which was partially offset by net proceeds from the issuance of 8.2 million shares of our common stock to employees as well as cash proceeds received from the sale of put warrants.

**EMPLOYEES** | The number of employees was 1,987 in 2001, 1,947 in 2000, and 1,398 in 1999, reflecting an increase of 2.1% in 2001 and 39.3% in 2000 from their respective preceding years.

**IMPACT OF CURRENCY TRANSLATION AND INFLATION** | We purchase the majority of our materials and services in U.S. dollars and transact our foreign sales in U.S. dollars. We have, in the past, entered into forward contracts to hedge against currency fluctuations associated with contractual commitments denominated in foreign currencies. During 2000, we entered into a forward exchange contract to purchase Malaysian ringgits to meet a portion of our firm contractual commitments to be paid in ringgits. The contract was settled in June 2001. As of December 31, 2001, we had no open forward contracts; however, we may enter into similar contracts from time to time to hedge foreign exchange exposure. To date, inflation has not significantly impacted our financial results; however, we cannot assure you that inflation will not affect us materially in the future.

**COMMON STOCK REPURCHASES** | During fiscal 2001, we repurchased a total of 7.2 million shares of common stock for an aggregate cost of \$183.2 million. During fiscal 2000, we repurchased a total of 17.1 million shares of common stock for an aggregate cost of \$555.5 million. During fiscal 1999, we repurchased a total of 4.3 million shares of common stock for an aggregate cost of \$87.1 million. As of December 31, 2001, 48.0 million shares were authorized for repurchase. Since the inception of the repurchase program in 1996 through December 31, 2001, we have repurchased a total of 37.1 million shares. All shares were retired upon acquisition.

**NEW ACCOUNTING PRONOUNCEMENTS** | In July 2001, the Financial Accounting Standards Board, or FASB, issued Statement of Financial Accounting Standards No. 141, or SFAS No. 141, "Business Combinations" and SFAS No. 142, "Goodwill and Other Intangible Assets." SFAS No. 141 requires that business combinations initiated after June 30, 2001 be accounted for under the purchase method of accounting.

SFAS No. 142 addresses how intangible assets shall be accounted for in financial statements upon their acquisition. Under SFAS No. 142, goodwill and other intangible assets deemed to have indefinite lives may not be amortized, but shall be reviewed and tested annually for impairment. SFAS No. 142 will be effective for fiscal years beginning after December 15, 2001. Our adoption of SFAS No. 142 on January 1, 2002 did not have a material effect on our financial statements.

In October 2001, the FASB issued SFAS No. 144, "Accounting for the Impairment or Disposal of Long-Lived Assets." SFAS No. 144 addresses financial accounting and reporting for the impairment of long-lived assets and for long-lived assets to be disposed, and requires that one accounting model be used for long-lived assets to be disposed of by sale, whether previously held and used or newly acquired. SFAS No. 144 will be effective for fiscal years beginning after December 15, 2001. Our adoption of SFAS No. 144 on January 1, 2002 did not have a material effect on our financial statements.

**FUTURE RESULTS; RISK FACTORS** | In addition to other information contained elsewhere in this Report, the following important factors, among others, have affected and, in the future, could affect our actual results of operations and could cause our actual results to differ materially from those expressed in forward-looking statements made by us.

*Our financial results depend on our ability to compete successfully in the highly competitive semiconductor industry.*

The programmable logic industry is intensely competitive. Future operating results will depend on our ability to develop, manufacture, and sell complex semiconductor components and programming software that offer customers greater value than solutions offered by competing vendors, including Xilinx and Lattice. We may not succeed in developing, manufacturing, or selling competitive products.

Because we develop PLDs for applications that are presently served by ASIC vendors, we also indirectly compete in the ASIC market. Many of these vendors have substantially greater financial, technical, and marketing resources than we do and have well-established market positions and solutions that have been proven technically feasible and economically competitive over several decades. We cannot assure you that we will be successful in displacing ASIC vendors in the targeted applications and densities. Furthermore, other programmable logic vendors are targeting these applications and may be successful in securing market share from us. Moreover, our customers increasingly use standard cell technologies to achieve greater integration in their systems; this may not only impede our efforts to penetrate the ASIC market, but may also displace our products in the applications that we presently serve.

*Our future success depends on our ability to define, develop, and sell new products.*

As a semiconductor company, we operate in a dynamic market characterized by rapid product obsolescence. We continue to focus our efforts on developing new PLDs, related development software and hardware, and advanced semiconductor wafer fabrication processes. We cannot assure you that we will be able to continue to develop and introduce new products and manufacturing processes, that our products will achieve market acceptance, or that our processes will be successful. If we do not successfully define, develop, and timely introduce competitive new products and enhance existing products in response to both evolving demands of the marketplace and competitive product offerings, our future operating results could be adversely affected.

*We depend on independent subcontractors, located primarily in Asia, for the supply and quality of our finished silicon wafers.*

We depend significantly upon subcontractors to manufacture our silicon wafers. Our primary wafer supply arrangements are with two semiconductor vendors: TSMC and Sharp. Although there is presently good availability in the silicon market generally and from TSMC and Sharp specifically, semiconductor foundry capacity can become limited quickly and without much notice. Furthermore, since only newer fabrication or substantially retrofitted facilities are able to manufacture wafers that incorporate leading-edge technologies, any significant decrease in capacity of these facilities could have a material adverse effect on our ability to obtain wafer supply for our newer products. Accordingly, we cannot assure you that any shortage in foundry manufacturing capacity will not result in production problems for us in the future.

In addition to sufficient foundry manufacturing capacity, we depend upon our foundry vendors to produce wafers at acceptable yields and to deliver them to us in a timely manner. Good production yields and timely delivery are necessary to meet customers' demand for products and to maintain profit margins. The manufacture of advanced CMOS wafers is a highly complex process. Wafer production yields are dependent on a wide variety of factors, including the level of contaminants in the manufacturing environment, impurities in the materials used, and the performance of personnel and equipment. As is common in the semiconductor industry, we have experienced, and may experience from time to time, problems with achieving acceptable production yields and timely delivery from our foundry vendors.

Difficulties in production yields can often occur when we begin production of new products, when we transition to new processes, or when our principal wafer supplier, TSMC, moves production of a product from one manufacturing plant to another, or manufactures the same product at multiple factories. These difficulties can potentially result in significantly higher costs and lower product availability. Although our inventory levels are currently ample relative to demand, we have in the past experienced shortages in supply. For example, from the fourth quarter of 1999 through the first half of 2000, process control issues associated with volume ramp up at a wafer supplier resulted in low die yields on FLEX 10KA and FLEX 10KE products,

thereby leading to reduced product availability in these families. As a result, we were unable to support distributor stocking at desired levels and in some cases could not meet end customer demand. Further, in the second quarter of 1999, difficulties with a vendor's manufacturing process limited the availability of packaging material (piece parts) used in certain of our new and proprietary FineLine BGA™, or ball-grid array, packages, thereby causing limited production. This in turn limited shipments of our new FLEX 10KE product family. Finally, production throughput times vary considerably among our wafer suppliers and among the various factories used by our wafer suppliers, and we may experience delays from time to time in processing some of our products, which also may result in higher costs and lower product availability.

Our management expects that, as is customary in the semiconductor business, to maintain or enhance our competitive position, we will continue to introduce new and established products using new and more advanced process technologies. For example, our Stratix family will be manufactured on a 0.13-micron, all-layer-copper interconnect process for which there is limited production history. We will also continue to transition our fabrication process arrangements to larger wafer sizes and smaller circuit geometries. Such transitions entail inherent technological risks and start-up difficulties that can adversely affect yields, costs, and time of delivery. To enhance our product designs and cost structure, we depend on all of our subcontractors, and especially our principal foundry partner, TSMC, to improve process technologies in a timely manner.

To ensure the continued supply of wafers, we may engage additional relationships and establish other sources of wafer supply for our products as such arrangements become economically advantageous or technically necessary. If we engage alternative sources of supply, we may encounter start-up difficulties. Also, shipments could be delayed significantly while such sources are qualified for volume production. Any significant delay caused by start-up difficulties or foundry qualification could have a material adverse effect on our operating results and cash flows.

Market conditions, including currency fluctuation, political strife, labor disruption, power shortages, and other factors, including natural or man-made disasters, adverse changes in tax laws, tariff, or freight rates, or interruption in air transportation, in areas where our foundry vendors are located also could have a severe negative impact on our operating capabilities. For example, in September 1999, a major earthquake struck Taiwan, resulting in widespread physical damage and loss of life. The earthquake halted wafer fabrication production at our primary vendor, TSMC, for several days and then only limited production began. Nearly two weeks passed before full production resumed, and a portion of the inventory in the production process was scrapped as a result of damage incurred during the earthquake.

*We depend on independent subcontractors, located primarily in Asia, for the testing and assembly of our semiconductor products.*

Independent subcontractors, located primarily in Asia, test and assemble our semiconductor products. Although these subcontractors have not recently experienced any serious work stoppages, the economic, social, and political situations in countries where certain subcontractors are located are unpredictable and can be volatile. Any unfavorable economic conditions, political strife, prolonged work stoppages, natural or man-made disasters, or power shortages in these countries, or other factors that could adversely affect the ability of our independent subcontractors to manufacture, test, and assemble our products would have a material adverse effect on our operating results and cash flows.

*We may be unable to adequately protect our intellectual property rights and may face significant future litigation expenses.*

We rely on patent, trademark, trade secret, copyright, and mask work laws to protect our intellectual property rights. We own numerous patents relating to various aspects of our products and technology and have a number of patent applications currently pending. Although our patents and patent applications may have value in discouraging competitive entry into our market segment, we cannot assure you that any valuable new patents will be granted to us, that our patents will provide meaningful protection from competition, or that we can rely on our intellectual property rights in developing additional products.

Also, in the normal course of business, we from time to time receive and make inquiries with respect to possible patent infringements. As a result of inquiries received from third parties, it may be necessary or desirable for us to obtain licenses relating to one or more of our current or future products. We cannot assure you that such licenses could be obtained, and, if obtainable, could be obtained on conditions that would not have a material adverse effect on our financial position or operating results.

Finally, we have been a party to lawsuits and may in the future become a party to lawsuits involving various types of claims, including, but not limited to, unfair competition and intellectual property matters. Legal proceedings tend to be unpredictable and costly and may be affected by events outside of our control. We cannot assure you that we will succeed in defending or enforcing our intellectual property rights. We also cannot assure you that third parties would not succeed in obtaining significant monetary damages or an injunction against the manufacture and sale of one or more of our product families, thereby adversely affecting our financial position or results of operations.

*We depend on independent distributors to generate sales and fulfill our customer orders.*

Worldwide sales through independent distributors accounted for over 97% of our total sales in 2001. We rely on a variety of independent distributors to assist us in creating customer demand, providing technical support and other value-added services to our customers, filling customer orders, and stocking our products. These distributors are located all over the world and are of various sizes and financial strength. We are highly dependent on Arrow in many locations across the world, particularly in North America where Arrow is our only distributor. While we have contractual relationships with all of our distributors, these contracts may be terminated by either party in a relatively short period of time. Any adverse impact on the ability of our independent distributors to assist us in marketing and selling our products for any reason would have a material adverse effect on our operating results and cash flows.

*We depend on international sales for a significant portion of our total sales.*

During each of the last two years, international sales constituted a significant portion of our total sales. In 2001, international sales constituted over 55% of our total sales. Risks related to our foreign operations include unfavorable economic conditions in a specific country or region, fluctuation in foreign currency exchange rates, foreign currency weakness against the U.S. dollar, adverse changes in tax laws, freight costs or interruptions in air transportation, reduced protection for intellectual property rights in some countries, generally longer receivable collection periods, and natural or man-made disasters in a specific country or region where we sell our products. Our business is also subject to the risks associated with the imposition of legislation and regulations relating specifically to the importation or exportation of semiconductor products. We cannot predict whether quotas, duties, tariffs, taxes, or other charges, restrictions, or trade barriers will be imposed by the United States or other countries upon the importation or exportation of our products in the future, or what, if any, effect such actions would have on our operating results.

*Our financial results are affected by the cyclical nature of the semiconductor industry.*

The semiconductor industry is highly cyclical. It is currently experiencing a significant downturn as a result of diminished demand for semiconductor products, excess production capacity, and accelerated declines in average selling prices. This economic downturn has reduced demand for our own products as well as raw materials and services provided by our key suppliers, thereby resulting in inventory charges of \$154.5 million in 2001 related primarily to excess inventory. The reduction in overall industry demand has financially stressed certain of our subcontractors and has weakened their capital structures. Currently, we do not expect any disruption to our supply chain due to this economic downturn. If these conditions in the semiconductor industry persist or worsen in the future, or if other unfavorable conditions occur, our future operating results could be further adversely affected.

*Our financial results are affected by general economic conditions.*

As a result of unfavorable economic conditions and reduced capital spending by our customers, our sales have decreased during 2001 compared to the same period a year ago. This downturn in customer demand resulted in excess inventory charges taken in 2001. Additionally, we significantly reduced factory activity, which resulted in under-absorbed manufacturing overhead. Anticipated declines in average selling prices, coupled with under-absorbed manufacturing overhead, have reduced, and may continue to reduce, gross margins. If economic conditions worsen, or if a wider economic slowdown occurs, our future operating results could be further adversely affected.

*Our quarterly operating results may fluctuate.*

Our quarterly operating results may fluctuate in the future as a result of a number of factors, including:

- The cyclical nature of the semiconductor industry
- The cyclical nature of demand for our customers' products
- General economic conditions in the countries where we sell our products
- Demand for our products
- The pricing of our products
- The timing of our and our competitors' new product introductions
- Our inventory levels and product obsolescence
- The scheduling, rescheduling, and cancellation of large orders by our customers
- The availability of adequate supply commitments from our wafer foundries and assembly and test subcontractors
- Our ability to develop new process technologies and achieve volume production at the foundries of TSMC or Sharp
- Changes in manufacturing yields
- Adverse movements in exchange rates, interest rates, or tax rates
- Litigation expenses incurred in connection with the defense of our intellectual property rights

*Our future success depends on our ability to successfully compete with other technology firms in attracting and retaining key technical and management personnel.*

Our future success depends, in large part, upon the continued service of our key management, technical, sales, and support employees, and on our ability to continue to attract and retain additional qualified employees. The competition for such employees is intense and the loss of key employees could have an adverse effect on our operating results.

*Our stock price may be subject to significant volatility.*

In recent years, the stock market has experienced extreme price volatility and the price of our common stock has been subject to wide fluctuations. The overall stock market, the prices of semiconductor stocks in general, and the price of our stock may continue to fluctuate greatly. We believe that factors such as quarter-to-quarter variances in financial results, announcements of new products, new orders, and order rate variations by us or our competitors could cause the market price of our common stock to fluctuate substantially. In addition, the stock prices for many high technology companies experience large fluctuations, which are often unrelated to the operating performance of the specific companies. Broad market fluctuations, as well as general economic conditions such as a recessionary period or high interest rates, may adversely affect the market price of our common stock.

#### ***Item 7A. Quantitative and Qualitative Disclosures about Market Risk.***

Our investment portfolio consisted of fixed income securities of \$738.3 million as of December 31, 2001 and \$1,028.8 million as of December 31, 2000. These securities, like all fixed income instruments, are subject to interest rate risk and will vary in value as market interest rates fluctuate. If market interest rates were to increase immediately and uniformly by 10% from levels as of December 31, 2001 and December 31, 2000, the decline in the fair value of the portfolio would not be material. Additionally, we anticipate holding our fixed income investments until maturity and, therefore, we do not expect to realize an adverse impact on income or cash flows.

We have international subsidiaries and branch operations and are, therefore, subject to foreign currency rate exposure. To date, our exposure to exchange rate volatility has not been significant. If foreign currency rates were to fluctuate by 10% from rates at December 31, 2001 and December 31, 2000, our financial position and results of operations would not be materially affected. However, we cannot assure you that there will not be a material impact in the future.

***Item 8. Financial Statements and Supplementary Data.***

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## Consolidated Balance Sheets

(In thousands, except par value amount)	December 31,	
	2001	2000
<b>ASSETS</b>		
Current assets:		
Cash and cash equivalents	\$ 145,048	\$ 496,385
Short-term investments	660,643	637,224
Total cash, cash equivalents, and short-term investments	805,691	1,133,609
Accounts receivable, less allowance for doubtful accounts of \$5,965 and \$5,998, respectively	33,931	168,940
Inventories	77,611	273,562
Deferred income taxes	125,672	178,750
Other current assets	86,443	14,498
Total current assets	1,129,348	1,769,359
Property and equipment, net	217,282	207,858
Investments and other assets	14,797	26,917
	<u>\$ 1,361,427</u>	<u>\$ 2,004,134</u>
<b>LIABILITIES AND STOCKHOLDERS' EQUITY</b>		
Current liabilities:		
Accounts payable	\$ 17,573	\$ 86,409
Accrued liabilities	26,644	26,992
Accrued compensation	22,102	46,144
Deferred income on sales to distributors	147,745	460,314
Income taxes payable	32,863	136,345
Total current liabilities	246,927	756,204
Commitments and contingencies (See Notes 9 and 13)		
Stockholders' equity:		
Common stock;		
\$.001 par value; 1,000,000 shares authorized; 386,301 and 389,265 shares issued and outstanding, respectively	386	389
Capital in excess of par value	394,748	389,184
Retained earnings	740,655	908,196
Deferred stock-based compensation	(24,961)	(49,101)
Accumulated other comprehensive income (loss)	3,672	(738)
Total stockholders' equity	1,114,500	1,247,930
	<u>\$ 1,361,427</u>	<u>\$ 2,004,134</u>

See accompanying notes to consolidated financial statements.

## Consolidated Statements of Operations

(In thousands, except per share amounts)	Years Ended December 31,		
	2001	2000	1999
Net sales	\$ 839,376	\$1,376,815	\$ 836,623
Cost of sales	458,699	466,994	301,322
Gross margin	380,677	909,821	535,301
Research and development expenses	170,869	172,373	86,065
Selling, general, and administrative expenses	215,318	209,979	143,214
Restructuring and other special charges	47,669	-	-
Acquired in-process research and development expense	-	6,305	-
Income (loss) from operations	(53,179)	521,164	306,022
Gain on sale of WaferTech, LLC	-	178,105	-
Interest and other income, net	40,176	46,145	37,055
Income (loss) before income taxes and equity investment	(13,003)	745,414	343,077
Provision for income taxes	26,779	247,107	111,499
Equity in loss of WaferTech, LLC	-	1,400	7,584
Net income (loss)	\$ (39,782)	\$ 496,907	\$ 223,994
Net income (loss) per share:			
Basic	\$ (0.10)	\$ 1.25	\$ 0.57
Diluted	\$ (0.10)	\$ 1.19	\$ 0.54
Shares used in computing per share amounts:			
Basic	386,097	396,849	396,158
Diluted	386,097	416,629	414,928

See accompanying notes to consolidated financial statements.

## Consolidated Statements of Cash Flows

(In thousands)	Years Ended December 31,		
	2001	2000	1999
Cash Flows from Operating Activities:			
Net income (loss)	\$ (39,782)	\$ 496,907	\$ 223,994
Adjustments to reconcile net income (loss) to net cash (used for) provided by operating activities:			
Depreciation and amortization	54,278	40,065	29,416
Amortization of deferred stock-based compensation	18,569	9,764	-
Deferred income taxes	50,383	(93,531)	(15,103)
Non-cash restructuring and other special charges	20,311	-	-
Write-off of acquired in-process research and development	-	6,305	-
Equity in loss of WaferTech, LLC	-	1,400	7,584
Gain on sale of WaferTech, LLC	-	(178,105)	-
Gain on sale of MAX 5000 product family	-	-	(10,275)
Changes in assets and liabilities:			
Accounts receivable, net	134,969	(78,839)	(33,963)
Inventories	195,951	(209,268)	5,375
Other current assets	(71,619)	9,449	19,232
Accounts payable and accrued liabilities	(93,233)	73,361	33,671
Deferred income on sales to distributors	(312,569)	232,554	66,425
Income taxes payable	(75,600)	240,353	76,423
Cash (used for) provided by operating activities	(118,342)	550,415	402,779
Cash Flows from Investing Activities:			
Purchases of property and equipment	(65,758)	(87,508)	(29,821)
Net change in short-term investments	(16,314)	42,976	(233,332)
Net change in other long-term investments	(2,000)	(4,000)	(1,928)
Proceeds from sale of WaferTech, LLC	-	350,384	-
Acquisitions of DesignPRO and Right Track	-	(11,535)	-
Investment in WaferTech, LLC	-	-	(60,500)
Proceeds from sale of MAX 5000 product family	-	-	10,700
Cash (used for) provided by investing activities	(84,072)	290,317	(314,881)
Cash Flows from Financing Activities:			
Net proceeds from issuance of common stock	34,311	39,871	29,945
Repurchase of common stock	(183,234)	(555,453)	(87,053)
Proceeds from sale of put warrants	-	6,978	2,438
Cash used for financing activities	(148,923)	(508,604)	(54,670)
Net (decrease) increase in cash and cash equivalents	(351,337)	332,128	33,228
Cash and cash equivalents at beginning of year	496,385	164,257	131,029
Cash and cash equivalents at end of year	\$ 145,048	\$ 496,385	\$ 164,257
Cash paid during the year for:			
Income taxes, net of refunds	\$ 122,907	\$ 106,777	\$ 45,335
Supplemental disclosure of non-cash activities:			
Issuance of common stock and options for acquisitions	-	59,928	2,927

See accompanying notes to consolidated financial statements.

# *Consolidated Statements of Stockholders' Equity*

(In thousands)	Number of Common Shares	Common Stock and Capital In Excess of Par Value	Retained Earnings	Deferred Stock-based Compensation	Accumulated Other Comprehensive Income (Loss)	Total Stockholders' Equity
Balance, December 31, 1998	390,540	\$ 314,280	\$ 567,441	\$ -	\$ -	\$ 881,721
Net income	-	-	223,994	-	-	223,994
Tax benefit resulting from employee stock transactions	-	64,101	-	-	-	64,101
Issuance of common stock	10,934	29,945	-	-	-	29,945
Issuance of common stock for acquisition	116	2,927	-	-	-	2,927
Repurchase of common stock	(4,330)	(87,053)	-	-	-	(87,053)
Proceeds from sales of put warrants	-	2,438	-	-	-	2,438
Balance, December 31, 1999	397,260	326,638	791,435	-	-	1,118,073
Components of comprehensive income:						
Net income	-	-	496,907	-	-	496,907
Unrealized loss on available-for-sale investments, net of tax benefit of \$472	-	-	-	-	(738)	(738)
Total comprehensive income	-	-	-	-	-	496,169
Tax benefit resulting from employee stock transactions	-	113,859	-	-	-	113,859
Issuance of common stock	8,201	39,871	-	-	-	39,871
Issuance of common stock and options for acquisitions	934	59,928	-	(41,259)	-	18,669
Deferred stock-based compensation resulting from issuance of restricted stock	-	17,606	-	(17,606)	-	-
Amortization of deferred stock-based compensation	-	-	-	9,764	-	9,764
Repurchase of common stock	(17,130)	(175,307)	(380,146)	-	-	(555,453)
Proceeds from sales of put warrants	-	6,978	-	-	-	6,978
Balance, December 31, 2000	389,265	389,573	908,196	(49,101)	(738)	1,247,930
Components of comprehensive loss:						
Net loss	-	-	(39,782)	-	-	(39,782)
Unrealized gain on available-for-sale investments, net of tax expense of \$2,695	-	-	-	-	4,410	4,410
Total comprehensive loss	-	-	-	-	-	(35,372)
Tax benefit resulting from employee stock transactions	-	27,882	-	-	-	27,882
Issuance of common stock	4,256	34,311	-	-	-	34,311
Deferred stock-based compensation resulting from issuance of restricted stock	-	283	-	(283)	-	-
Amortization of deferred stock-based compensation	-	-	-	18,569	-	18,569
Reversal of deferred stock-based compensation due to forfeitures	-	(1,440)	-	1,440	-	-
Write-off of deferred stock-based compensation related to restructuring	-	-	-	4,414	-	4,414
Repurchase of common stock	(7,220)	(55,475)	(127,759)	-	-	(183,234)
Balance, December 31, 2001	386,301	\$ 395,134	\$ 740,655	\$ (24,961)	\$ 3,672	\$ 1,114,500

See accompanying notes to consolidated financial statements.

## *Notes to the Consolidated Financial Statements*

### **Note 1: The Company**

Altera Corporation was founded in 1983 and reincorporated in the State of Delaware in 1997. We design, manufacture, and market high-performance, high-density programmable logic devices, or PLDs, intellectual property cores, and associated development tools. PLDs are semiconductor chips that can be programmed on-site using software tools that run on personal computers or engineering workstations. User benefits include ease of use, lower risk, and fast time-to-market. Our products serve a wide range of markets, including telecommunication, data communication, electronic data processing, computer peripheral, and industrial applications.

### **Note 2: Significant Accounting Policies**

**BASIS OF PRESENTATION** | We have a fiscal year that ends on the Friday nearest December 31st. For presentation purposes, the consolidated financial statements and accompanying notes refer to our fiscal year end as December 31st. The consolidated financial statements include our accounts as well as our wholly-owned subsidiaries after elimination of all significant intercompany balances and transactions.

**USE OF ESTIMATES** | The preparation of financial statements in conformity with accounting principles generally accepted in the United States of America requires management to make estimates and assumptions that affect the reported amounts of assets and liabilities and disclosure of contingent assets and liabilities at the date of the financial statements and the reported amounts of revenues and expenses during the reporting period. Actual results could differ from those estimates, and material effects on our operating results and financial position may result.

**CASH EQUIVALENTS AND SHORT-TERM INVESTMENTS** | Cash equivalents consist of highly liquid investments with original maturities of three months or less. Short-term investments are held as securities available for sale and are carried at their market value based on quoted market prices as of the balance sheet date. The amortized cost of securities is adjusted for amortization of premiums and accretion of discounts to maturity. Such amortization is included in investment income. Realized gains or losses are determined on the specific identification method and are reflected in income. Net unrealized gains or losses are recorded directly in stockholders' equity except those unrealized losses that are deemed to be other than temporary are reflected in income.

**INVENTORIES** | Inventories are recorded at the lower of standard cost, which approximates actual cost on a first-in-first-out basis, or market value. The inventories at December 31, 2001 and 2000 were comprised of the following:

(In thousands)	December 31,	
	2001	2000
Raw materials and work in process	\$ 50,417	\$ 203,681
Finished goods	27,194	69,881
Total inventories	\$ 77,611	\$ 273,562

As a result of unfavorable economic conditions and diminished demand for semiconductor products, we experienced a sharp decline in sales and recorded inventory charges of \$154.5 million in 2001. These inventory charges, which were recorded in cost of sales in our consolidated statement of operations, related primarily to excess inventory for our APEX 20KE, FLEX 10KE, and MAX 7000A product families and assembly package material.

**PROPERTY AND EQUIPMENT** | Property and equipment are carried at cost less accumulated depreciation and amortization. Depreciation and amortization are computed using the straight-line method. Estimated useful lives of three to five years are used for equipment and office furniture and forty years for buildings. Amortization of leasehold improvements is computed using the shorter of the remaining facility lease term or the estimated useful life of the improvements. Property and equipment at December 31, 2001 and 2000 was comprised of the following components:

(In thousands)	December 31,	
	2001	2000
Land	\$ 30,779	\$ 30,474
Building	118,785	89,419
Equipment and software	193,592	183,315
Office furniture and fixtures	19,930	17,392
Leasehold improvements	4,980	3,190
Property and equipment, at cost	368,066	323,790
Accumulated depreciation and amortization	(150,784)	(115,932)
Property and equipment, net	\$ 217,282	\$ 207,858

We evaluate the recoverability of our property and equipment and intangible assets in accordance with SFAS No. 121, "Accounting for the Impairment of Long-Lived Assets and for Long-Lived Assets to be Disposed of." This standard requires recognition of impairment of long-lived assets in the event the carrying value of such assets exceeds the future undiscounted cash flows attributable to such assets. On January 1, 2002, SFAS No. 144, "Accounting for the Impairment or Disposal of Long-Lived Assets" became effective. This standard supersedes SFAS No. 121 and requires that one accounting model be used for long-lived assets to be disposed of by sale, whether previously held and used or newly acquired. Our adoption did not have a material effect on our financial statements.

**FAIR VALUE OF FINANCIAL INSTRUMENTS** | For certain of our financial instruments, including cash and cash equivalents, short-term investments, accounts receivable, accounts payable, and accrued liabilities, the carrying amounts approximate fair value due to their short maturities.

**CONCENTRATIONS OF CREDIT RISK** | Financial instruments that potentially subject us to concentrations of credit risk consist principally of cash, cash equivalents, short-term investments, and accounts receivable. We place our cash, cash equivalents, and short-term investments in a variety of financial instruments and, by policy, limit the amount of credit exposure through diversification and by restricting our investments to highly rated securities.

We sell our products to distributors and OEMs throughout the world. We perform ongoing credit evaluations of our customers' financial condition and generally require collateral whenever deemed necessary. For the year ended December 31, 2001, worldwide sales through distributors accounted for over 97% of total sales, and Arrow was, and continues to be, our largest distributor. In 2001 and 2000, two distributors accounted for more than 10% of sales. In 2001, one distributor accounted for 54% of sales, and the other distributor accounted for 13% of sales. In 2000, one distributor accounted for 58% of sales, and the other distributor accounted for 11% of sales. In 1999, three distributors accounted for more than 10% of sales. These three distributors accounted for 34%, 19%, and 13% of sales. The percentage increases for our largest distributor in 2001 and 2000 compared to 1999 are attributable to the combination of Arrow and Wyle Electronics, our two largest distributors in 2000. For the years ended December 31, 2001, 2000, and 1999, no single end customer provided more than 10% of our sales.

At December 31, 2001, three distributors, each of which accounted for more than 10% of total accounts receivable, accounted for 42%, 24%, and 12% of total accounts receivable. At December 31, 2000, one distributor accounted for 45% of total accounts receivable.

**FOREIGN EXCHANGE CONTRACTS** | We purchase the majority of our materials and services in U.S. dollars and transact our foreign sales in U.S. dollars. We have, in the past, entered into forward contracts to hedge against currency fluctuations associated with contractual commitments denominated in foreign currencies. During 2000, we entered into a forward exchange contract to purchase Malaysian ringgits to meet a portion of our firm contractual commitments to be paid in ringgits. The

contract was settled in June 2001. As of December 31, 2001, we had no open forward contracts; however, we may enter into similar contracts from time to time to hedge foreign exchange exposure.

**REVENUE RECOGNITION** | We recognize revenue from product sales upon shipment to OEMs and end users provided that persuasive evidence of an arrangement exists, the price is fixed, title has transferred, collection of resulting receivables is reasonably assured, there are no customer acceptance requirements, and there are no remaining significant obligations. Reserves for sales returns and allowances are recorded at the time of shipment. Our sales to distributors are made under agreements allowing for returns or credits under certain circumstances. We defer recognition of revenue on sales to distributors until products are resold by the distributor to the end user.

**DEPENDENCE ON WAFER SUPPLIERS AND OTHER INDEPENDENT SUBCONTRACTORS** | We do not directly manufacture finished silicon wafers. Our strategy has been to purchase silicon wafers from independent wafer foundries. We also depend on these wafer foundries to improve process technologies in a timely manner and to enhance our product designs and cost structure. Although there is presently good availability in the silicon market, semiconductor foundry capacity can become limited quickly and without much notice. We cannot assure you that any future shortage in foundry manufacturing capacity will not result in production problems for us in the future.

We also depend on independent subcontractors, located primarily in Asia, for the testing and assembly of our semiconductor products. Any unfavorable economic conditions, political strife, prolonged work stoppages, natural or man-made disasters, or power shortages in these countries, or other factors, may adversely affect the ability of our independent subcontractors to manufacture, test, and assemble our products, and therefore may have a material adverse effect on our operating results, financial position, and cash flows.

**STOCK-BASED COMPENSATION PLANS** | We account for stock-based compensation using the intrinsic value method prescribed in Accounting Principles Board Opinion No. 25, or APB No. 25, "Accounting for Stock Issued to Employees." Under APB No. 25, compensation cost is measured as the excess, if any, of the quoted market price of our stock at the date of grant over the exercise price of the option granted. Compensation cost for stock options, if any, is recognized ratably over the vesting period. We provide additional pro forma disclosures as required under SFAS No. 123, "Accounting for Stock-Based Compensation."

**FOREIGN CURRENCY TRANSLATION** | The U.S. dollar is the functional currency for each of our foreign subsidiaries. Assets and liabilities that are not denominated in the functional currency are remeasured into U.S. dollars and the resulting gains or losses are included in "Interest and other income, net."

**NEW ACCOUNTING PRONOUNCEMENTS** | In July 2001, the FASB issued SFAS No. 141, "Business Combinations" and SFAS No. 142, "Goodwill and Other Intangible Assets." SFAS No. 141 requires that business combinations initiated after June 30, 2001 be accounted for under the purchase method of accounting.

SFAS No. 142 addresses how intangible assets shall be accounted for in financial statements upon their acquisition. Under SFAS No. 142, goodwill and other intangible assets deemed to have indefinite lives may not be amortized, but shall be reviewed and tested annually for impairment. SFAS No. 142 will be effective for fiscal years beginning after December 15, 2001. Our adoption of SFAS No. 142 on January 1, 2002 did not have a material effect on our financial statements.

In October 2001, the FASB issued SFAS No. 144, "Accounting for the Impairment or Disposal of Long-Lived Assets." SFAS No. 144 addresses financial accounting and reporting for the impairment of long-lived assets and for long-lived assets to be disposed, and requires that one accounting model be used for long-lived assets to be disposed of by sale, whether previously held and used or newly acquired. SFAS No. 144 will be effective for fiscal years beginning after December 15, 2001. Our adoption of SFAS No. 144 on January 1, 2002 did not have a material effect on our financial statements.

### **Note 3: Restructuring and Other Special Charges**

During 2001, we recorded restructuring and other special charges of \$47.7 million in connection with our plan to align our organization's cost structure with projected sales resulting from the unfavorable economic conditions and to reduce future operating expenses. This restructuring program includes a worldwide workforce reduction, the spin-off of Northwest Logic, the

write-down of certain equipment and intangible assets, the consolidation of excess facilities, and the termination of certain license agreements. In addition, we settled our patent litigation with Xilinx. These charges were classified as operating expenses in our consolidated statements of operations.

A summary of the restructuring and other special charges is as follows:

(In thousands)	Total Charges	Non-cash Charges	Cash Payments	Restructuring Liability as of December 31, 2001
Workforce reduction	\$ 3,834	\$ 83	\$ 2,900	\$ 851
Litigation settlement	20,000	-	20,000	-
Spin-off of Northwest Logic	6,697	6,338	200	159
Impairment of production and other equipment	8,158	8,158	-	-
Impairment of investments and intangible assets	5,157	5,157	-	-
Consolidation of excess facilities and other	3,823	575	2,031	1,217
Total	\$ 47,669	\$ 20,311	\$ 25,131	\$ 2,227

#### *Workforce Reduction*

We reduced our worldwide workforce by approximately 152 employees primarily in administrative functions located mainly in our headquarters facility in San Jose, California. The workforce reduction resulted in a \$3.8 million charge relating primarily to severance and fringe benefits. Additionally, we initiated cost reduction measures, which included a temporary reduction of executive officer pay by 10% and the cancellation of employee merit increases. We also reduced the number of temporary and contract workers and, starting in the first quarter of 2001, did not replace voluntary attrition except for key positions.

#### *Litigation Settlement*

In connection with the settlement of litigation with Xilinx, we entered into a royalty-free patent cross license agreement and agreed to make a one-time payment of \$20.0 million. Both companies also agreed to refrain from instituting further patent litigation between our two companies for the next five years.

#### *Spin-Off of Northwest Logic*

We completed the spin-off of Northwest Logic to two of its employees in December 2001. Northwest Logic was a design service center that we acquired in 2000. The spin-off resulted in the termination of 14 employees. We recorded a charge of \$6.7 million related primarily to stock-based compensation of \$4.3 million for the acceleration of unvested stock options of terminated employees, as well as severance, fringe benefits, and the write-off of certain tangible and intangible assets and liabilities relating to Northwest Logic.

#### *Impairment Loss on Equipment, Investments, and Intangible Assets*

We recorded a charge of \$8.2 million for the impairment of production and other equipment that has been abandoned or is being held for sale. Certain production equipment is now surplus to our requirements and marketed for sale. We reclassified \$1.4 million from property and equipment to other current assets in our consolidated balance sheet to reflect our intention to sell these assets within the next twelve months. The amount reclassified represents the estimated net realizable value of equipment that is being held for sale. We also recorded a \$5.2 million charge resulting from the impairment of purchased intangible assets related to technology acquired in previous acquisitions but no longer being used, as well as investments in development stage enterprises that are in financial difficulties.

### *Consolidation of Excess Facilities and Other*

We recorded a charge of \$3.8 million resulting from the consolidation of excess facilities primarily related to lease terminations and non-cancelable lease costs, as well as other charges including the termination of certain license agreements.

We substantially completed the implementation of our restructuring program in 2001. Amounts related to the termination of agreements and non-cancelable leases will be paid over their respective terms through the third quarter of 2005. Cash expenditures relating to workforce reductions will be paid by the first half of 2003. The restructuring liability, totaling \$2.2 million as of December 31, 2001, is included in accrued liabilities in the consolidated balance sheet.

#### **Note 4: Income Per Share**

Basic income (loss) per share is computed by dividing net income (loss) available to common stockholders by the weighted average number of common shares outstanding during the period and excludes the dilutive effect of stock options and restricted stock. Diluted income per share reflects the dilution of potential common shares outstanding during a period. In computing diluted income per share, the tax benefit resulting from employee stock transactions, unamortized deferred stock-based compensation, and the average stock price for the period are used in determining the number of shares assumed to be repurchased with the proceeds from the exercise of stock options.

Diluted loss per share excludes stock options and unvested restricted stock totaling 25.5 million shares for the year ended December 31, 2001, as their effect is antidilutive. These options, however, could be dilutive in the future. For the years ended December 31, 2000 and December 31, 1999, the excluded shares were immaterial. A reconciliation of basic and diluted income (loss) per share is presented below:

(In thousands, except per share amounts)	Years Ended December 31,		
	2001	2000	1999
Basic:			
Net income (loss)	\$ (39,782)	\$ 496,907	\$ 223,994
Weighted shares outstanding	386,097	396,849	396,158
Net income (loss) per share	\$ (0.10)	\$ 1.25	\$ 0.57
Diluted:			
Net income (loss)	\$ (39,782)	\$ 496,907	\$ 223,994
Weighted shares outstanding	386,097	396,849	396,158
Effect of dilutive securities:			
Stock options and restricted stock	-	19,780	18,770
	386,097	416,629	414,928
Net income (loss) per share	\$ (0.10)	\$ 1.19	\$ 0.54

## Note 5: Marketable Securities

Our portfolio of marketable securities at December 31 consists of the following:

(In thousands)	2001				2000			
	Cost	Gross Unrealized Gains	Gross Unrealized Losses	Fair Value	Cost	Gross Unrealized Gains	Gross Unrealized Losses	Fair Value
Money market funds	\$ 159	\$ -	\$ -	\$ 159	\$ 46,128	\$ -	\$ -	\$ 46,128
Municipal bonds	363,130	2,106	(124)	365,112	475,025	537	(80)	475,482
U.S. government and agency obligations	56,451	740	(87)	57,104	133,973	208	(29)	134,152
Corporate bonds	179,326	3,238	-	182,564	213,847	662	(2,687)	211,822
Other debt securities	133,329	51	(29)	133,351	161,050	187	(8)	161,229
Total	<u>\$ 732,395</u>	<u>\$ 6,135</u>	<u>\$ (240)</u>	<u>\$ 738,290</u>	<u>\$1,030,023</u>	<u>\$ 1,594</u>	<u>\$ (2,804)</u>	<u>\$1,028,813</u>

Included in:

Cash and cash equivalents	\$ 77,647	\$ 391,589
Short-term investments	660,643	637,224
Total	<u>\$ 738,290</u>	<u>\$1,028,813</u>

Our portfolio of marketable securities by contractual maturity at December 31 is as follows (in thousands):

	2001	2000
Due in one year or less	\$ 192,631	\$ 423,984
Due after one year through two years	545,659	604,829
Total	<u>\$ 738,290</u>	<u>\$1,028,813</u>

## Note 6: Acquisitions

We completed the acquisitions of all outstanding capital stock of DesignPRO Inc., a developer and provider of intellectual property cores and custom design solutions, on April 19, 2000, Right Track CAD Inc., a developer of architectural and computer aided design tools for advanced PLDs, on May 1, 2000, and Northwest Logic, Inc., a provider of system design services and intellectual property specializing in telecommunications, data communications, and embedded processor systems design, on September 11, 2000. Northwest Logic was subsequently spun-off in December 2001.

We issued 934,381 shares of our common stock and paid approximately \$11.5 million in cash, net of cash acquired of \$0.3 million, for all of the capital stock of DesignPRO, Right Track, and Northwest Logic. In addition, we granted options to purchase 323,146 shares of our common stock in exchange for all of the stock options outstanding of DesignPRO and Right Track. The fair value of our shares issued was approximately \$45.3 million and the fair value of our options granted was approximately \$14.6 million. Certain shares issued are subject to our repurchase rights under certain circumstances. We incurred direct acquisition costs of approximately \$0.4 million, which were included in the purchase price. Total consideration for the three acquisitions was \$72.1 million. The acquisitions were accounted for under the purchase method of accounting. The purchase price was allocated to the tangible and intangible assets acquired and liabilities assumed based in part on an independent appraisal of their respective fair values. Total consideration paid in connection with the acquisitions was attributable to the following:

(In thousands)	Amount	Amortization Period
Deferred stock-based compensation	\$ 41,259	2 to 4 years
Market ready technology	21,446	3 to 6 years
In-process research and development	6,305	-
Other intangible assets	2,481	3 years
Tangible assets and working capital	590	-
Total	<u>\$ 72,081</u>	

No supplemental pro forma information is presented due to the immaterial effect on prior period results of operations. The allocation of amounts to market ready technology and in-process research and development were consistent with widely recognized appraisal practices. Our analysis resulted in a valuation of market ready technology at \$21.4 million. Market ready technology represents technologies that have reached technological feasibility, and therefore can be capitalized. We are amortizing the market ready technology on a straight-line basis over a period of three to six years. Our analysis also resulted in a \$6.3 million charge to acquired in-process research and development. The acquired in-process technology represents the appraised value of technologies in the development stage that had not yet reached technological feasibility and do not have alternative future uses. We expensed this amount as a non-recurring charge upon consummation of the acquisitions.

We determined the value assigned to in-process research and development by identifying research projects in areas for which technological feasibility had not been established. For both the Right Track and DesignPRO valuations, we estimated the expected cash flows from the projects once commercially viable. We then discounted the net cash flows back to their present value and applied a percentage of completion. We determined the percentage of completion using milestones representing our management's estimate of effort, value added, and degree of difficulty of the portion of each project completed as of the acquisition date, as compared to the remaining research and development to be completed to bring each project to technical feasibility.

If we do not successfully develop our research projects discussed above, our sales and profitability may be adversely affected in future periods and the value of other intangible assets acquired may become impaired. Our management believes that the in-process research and development charge is valued consistently with the SEC staff's current views regarding valuation methodologies. We cannot assure you that the SEC staff will not take issue with any assumptions used in our valuation model and require us to revise the amount allocated to in-process research and development. As of December 31, 2001, we believe that the projections used in the valuations with respect to each acquisition are still materially valid; however, there can be no assurance that the projected results will be achieved.

As part of the restructuring program in 2001, we concluded the spin-off of Northwest Logic in December 2001. We also recorded a charge for the impairment of certain other purchased intangible assets. See Note 3.

#### **Note 7: Joint Venture**

In June 1996, we formed WaferTech, a joint venture company, with TSMC and several other partners to build and operate a wafer manufacturing plant in Camas, Washington. On December 27, 2000, we sold our 23% ownership interest in WaferTech to a subsidiary of TSMC for \$350.4 million in cash. The one-time pre-tax gain on the sale was \$178.1 million. Although we sold our equity interest in WaferTech in December 2000, we continue to utilize WaferTech as one of our suppliers of silicon wafers. Through December 27, 2000, we accounted for our investment under the equity method based on our ability to exercise significant influence over WaferTech's operating and financial policies. Our equity in the loss of WaferTech was \$1.4 million for 2000 and \$7.6 million for 1999.

#### **Note 8: Investments and Other Assets**

At December 31, 2001, our long-term investments and other assets of \$14.8 million consisted primarily of intangible assets acquired in connection with the acquisition of Right Track of approximately \$12.4 million, net of \$5.2 million of accumulated amortization. It also included certain equity investments accounted for under the cost method. At December 31, 2000, our long-term investments and other assets primarily consisted of intangible assets acquired in connection with the acquisitions of

DesignPRO, Right Track, and Northwest Logic of approximately \$21.1 million, net of \$2.9 million of accumulated amortization. As part of the restructuring program in 2001, we spun-off our Northwest Logic subsidiary in December 2001. We also recorded a charge for the impairment of certain other intangible assets and investments.

#### **Note 9: Commitments**

We lease certain of our sales facilities under non-cancelable lease agreements expiring at various times through 2009. The leases require us to pay property taxes, insurance, maintenance, and repair costs. Future minimum lease payments under all non-cancelable operating leases are as follows:

Years ending December 31,	(In thousands)
2002	\$ 6,041
2003	5,013
2004	4,289
2005	3,875
2006	2,186
Thereafter	4,304
Total	<u>\$ 25,708</u>

We have the option to extend or renew most of our leases. Rental expense under all operating leases amounted to \$5.9 million in 2001, \$3.5 million in 2000, and \$2.8 million in 1999.

#### **Note 10: Stockholders' Equity**

In May 2001, our stockholders voted to approve an amendment to our Certificate of Incorporation to increase the number of authorized shares from 700 million to 1 billion.

**COMMON STOCK REPURCHASES** | During fiscal 2001, we repurchased a total of 7.2 million shares of common stock for an aggregate cost of \$183.2 million. During fiscal 2000, we repurchased a total of 17.1 million shares of common stock for an aggregate cost of \$555.5 million. During fiscal 1999, we repurchased a total of 4.3 million shares of common stock for an aggregate cost of \$87.1 million. As of December 31, 2001, 48.0 million shares were authorized for repurchase. Since the inception of the repurchase program in 1996 through December 31, 2001, we have repurchased a total of 37.1 million shares. All shares were retired upon acquisition.

**PUT WARRANTS** | In December 1999 and June 2000, we sold put warrants to independent third parties. These put warrants entitled the holders the right to sell 2.5 million shares of our common stock to us at specified prices on stated maturity dates. The cash proceeds from the sale of the put warrants of \$7.0 million in 2000 and \$2.4 million in 1999 have been included as an addition to capital in excess of par value. During 2000, warrants for 1.5 million shares expired unexercised, while warrants for 1.0 million shares were exercised. We repurchased these 1.0 million shares for an aggregate cost of \$33.7 million. These shares were included in the 37.1 million total repurchased shares, which count against the 48.0 million shares authorized for repurchase under our common stock repurchase program.

**DEFERRED STOCK-BASED COMPENSATION** | During 2001, we recorded aggregate deferred stock-based compensation of \$283,000 representing the value of restricted stock issued to a new employee. During 2000, we recorded aggregate deferred stock-based compensation of \$58.9 million representing the value of restricted stock issued in conjunction with the acquisitions of DesignPRO and Right Track as well as stock options and restricted stock granted to certain new employees. Deferred stock-based compensation represents the difference between the grant price and the quoted market price of our stock at the date of grant. We are amortizing deferred stock-based compensation over the vesting period of three to four years. Amortization of deferred stock-based compensation was \$18.6 million during 2001 and \$9.8 million during 2000.

The restricted stock issued is subject to our repurchase rights under certain circumstances. These rights lapse over a three- to four-year period. During 2001, we repurchased 40,000 shares of restricted stock. At December 31, 2001, 737,342 shares were subject to our repurchase rights.

## Note 11: Stock-Based Compensation Plans

At December 31, 2001, we had three stock-based compensation plans, which are described below. We apply APB No. 25 in accounting for our plans.

**STOCK OPTION PLANS** | As of December 31, 2001, the 1996 Stock Option Plan had 59.0 million shares reserved for issuance and 7.8 million shares were available for future grants. The 1998 Director Stock Option Plan had 680,000 shares reserved for issuance and 415,000 shares were available for future grants.

Any shares reserved for issuance under the 1987 Stock Option Plan and the 1988 Director Stock Option Plan relating to ungranted stock options were canceled upon the adoption of the new option plans. As of December 31, 2001, under the 1987 Stock Option Plan, 7.3 million previously granted shares remained unexercised, while under the 1988 Director Stock Option Plan, 1.1 million previously granted shares remained unexercised.

The 1996 Stock Option Plan provides for the periodic issuance of stock options to our employees. Options granted under this plan will generally vest over four years at annual increments as determined by the Board of Directors. All options under this plan have a maximum term of 10 years.

The 1998 Director Stock Option Plan provides for the periodic issuance of stock options to members of our Board of Directors who are not employees. In March 2001, the Board of Directors approved an amendment to the vesting period for grants under this plan. For any new director elected to the board, the first grant vests over four years, the next three subsequent grants vest over a one-year period after the first grant is fully vested, and all subsequent grants vest over the year following the date of grant. For current board members, this amendment to the vesting period applies to all future grants. Options granted prior to March 2001 generally vest over four years. All options under this plan have a maximum term of 10 years.

A summary of our stock option activity and related weighted average exercise prices for the years ended December 31 is as follows:

(In thousands, except price per share amounts)	2001		2000		1999	
	Shares	Price	Shares	Price	Shares	Price
Options outstanding at beginning of year	50,681	\$ 16.52	46,778	\$ 9.06	50,948	\$ 5.45
Stock options:						
Granted	12,119	25.71	13,406	35.92	9,124	20.96
Exercised	(3,669)	5.98	(7,386)	4.13	(10,276)	2.23
Forfeited	(3,089)	29.55	(2,117)	17.74	(3,018)	7.39
Options outstanding at end of year	56,042	\$ 18.48	50,681	\$ 16.52	46,778	\$ 9.06

Range of Exercise Prices	Options Outstanding			Options Exercisable	
	Number Outstanding at 12/31/01 (In thousands)	Weighted Average Remaining Contractual Life (Years)	Weighted Average Exercise Price	Number Exercisable at 12/31/01 (In thousands)	Weighted Average Exercise Price
\$ 0.01 - \$ 6.63	10,477	3.33	\$ 3.62	10,317	\$ 3.68
\$ 6.64 - \$ 8.75	11,430	5.54	8.12	7,422	8.14
\$ 8.77 - \$ 22.49	13,237	8.19	18.52	2,260	14.81
\$ 22.63 - \$ 27.81	10,094	8.65	24.34	1,637	25.06
\$ 27.84 - \$ 46.22	9,355	9.00	35.86	629	37.20
\$ 46.31 - \$ 63.44	1,449	8.59	54.03	550	53.94
	56,042	6.97	\$ 18.48	22,815	\$ 9.90

Options exercisable as of December 31, 2000 were 15.9 million at an average price of \$5.86. Options exercisable as of December 31, 1999 were 15.4 million at an average price of \$3.80.

**EMPLOYEE STOCK PURCHASE PLAN** | As of December 31, 2001, the 1987 Employee Stock Purchase Plan had 14.2 million shares of common stock reserved for issuance. Under the terms of the Employee Stock Purchase Plan, our employees, nearly all of whom are eligible to participate, can choose each year to have up to 10% of their eligible annual base earnings withheld, up to a maximum of \$21,250, to purchase our common stock. Effective October 2001, the offering period was increased from six to twelve months. The purchase price of the stock is 85% of the lower of the closing price at the beginning of the twelve month offering period or at the end of each six-month purchase period. We do not recognize compensation cost related to employee purchase rights under this plan.

Sales under the Employee Stock Purchase Plan were 616,364 shares of common stock at an average price of \$20.06 per share in 2001, 423,988 shares at \$22.05 per share in 2000, and 634,478 shares at \$10.81 per share in 1999. There were 1.2 million shares available for future purchases under the Employee Stock Purchase Plan as of December 31, 2001.

We received tax benefits of \$27.9 million in 2001, \$113.9 million in 2000, and \$64.1 million in 1999 on the exercise of non-qualified stock options and on the disposition of stock acquired by exercise of incentive stock options or through the Employee Stock Purchase Plan.

**PRO FORMA NET INCOME AND NET INCOME PER SHARE** | The fair value of each option grant, as defined by SFAS No. 123, is estimated on the date of grant using the Black-Scholes option-pricing model. The Black-Scholes model, as well as other currently accepted option valuation models, was developed to estimate the fair value of freely tradable, fully transferable options without vesting restrictions that significantly differ from our stock option awards. These models also require highly subjective assumptions, including future stock price volatility and expected time until exercise, which greatly affect the fair value on the grant date.

To compute the estimated fair value of our stock option grants and shares purchased under the Employee Stock Purchase Plan, the Black-Scholes method was used with the following weighted-average assumptions and dividend yields of 0% for all years presented:

Years ended December 31,	Stock Options			Employee Stock Purchase Plan		
	2001	2000	1999	2001	2000	1999
Expected life from vesting date (years)	1.01	0.96	0.83	0.50	0.50	0.50
Expected stock price volatility	63.8%	57.3%	53.2%	91.5%	84.6%	45.9%
Risk-free interest rate	4.4%	6.2%	5.7%	3.9%	5.9%	4.5%

The estimated weighted-average fair value of options granted was \$13.94 in 2001, \$19.06 in 2000, and \$10.12 in 1999. The estimated weighted-average fair value of shares purchased under the Employee Stock Purchase Plan was \$10.50 in 2001, \$14.65 in 2000, and \$4.04 in 1999.

Had we recorded compensation costs based on the estimated grant date fair value as defined by SFAS No. 123, for awards granted under its Stock Option Plans and Stock Purchase Plan, our net income (loss) and net income (loss) per share would have been reduced to the pro forma amounts below for the years ended December 31, 2001, 2000, and 1999:

(In thousands, except per share amounts)	2001	2000	1999
Pro forma net income (loss)	\$ (123,824)	\$ 440,513	\$ 199,850
Pro forma net income (loss) per share:			
Basic	\$ (0.32)	\$ 1.11	\$ 0.50
Diluted	(0.32)	1.07	0.49

## Note 12: Income Taxes

U.S. and foreign components of income (loss) before income taxes were:

(In thousands)	Years Ended December 31,		
	2001	2000	1999
United States	\$ 643	\$ 619,032	\$ 280,254
Foreign	(13,646)	126,382	62,823
Income (loss) before income taxes	\$ (13,003)	\$ 745,414	\$ 343,077

Unremitted earnings of our foreign subsidiaries that are considered permanently invested outside the United States and on which no U.S. taxes have been provided, aggregate to approximately \$80.7 million at December 31, 2001.

The provision for income taxes consists of:

(In thousands)	Years Ended December 31,		
	2001	2000	1999
Current tax expense:			
United States	\$ (25,468)	\$ 282,547	\$ 113,510
State	-	29,454	15,365
Foreign	1,864	20,075	6,793
Total current tax (benefit) expense	(23,604)	332,076	135,668
Deferred taxes:			
United States	63,568	(64,892)	(18,064)
State	(3,368)	(10,481)	(4,552)
Foreign	(9,817)	(9,596)	(1,553)
Total deferred taxes	50,383	(84,969)	(24,169)
Total provision for income taxes	\$ 26,779	\$ 247,107	\$ 111,499

Deferred tax assets (liabilities) were as follows:

(In thousands)	December 31,	
	2001	2000
Assets:		
Accrued expenses and reserves	\$ 80,430	\$ 168,776
Net operating loss	18,488	-
Acquisition costs	15,638	6,084
Deferred compensation	14,375	10,990
Other	6,349	1,235
Gross deferred tax assets	135,280	187,085
Depreciation	(7,239)	(5,032)
Deferred tax asset valuation allowance	(2,369)	(3,303)
Net deferred tax assets	\$ 125,672	\$ 178,750

The valuation allowances of \$2.4 million at December 31, 2001, and \$3.3 million at December 31, 2000 are attributable to acquired intangible assets. Sufficient uncertainty exists regarding the realizability of these assets and, accordingly, valuation allowances are required.

At December 31, 2001, income tax receivable of \$73.2 million is classified as other current assets in our consolidated balance sheets.

The exercise of non-qualified stock options and the disposition of stock acquired by exercise of incentive stock options or through the Employee Stock Purchase Plan resulted in a tax benefit of \$27.9 million in 2001, \$113.9 million in 2000, and \$64.1 million in 1999. We receive an income tax benefit calculated as the tax effect of the difference between the fair market value of the stock issued at the time of exercise and the option price. These benefits are credited directly to stockholders' equity.

The items accounting for the difference between income taxes computed at the federal statutory rate and the provision for income taxes are as follows:

(In thousands)	Years Ended December 31,		
	2001	2000	1999
Tax provision (benefit) at U.S. statutory rates	\$ (4,551)	\$ 260,895	\$ 120,077
State taxes, net of federal benefit	(351)	20,872	8,920
Foreign income taxed at lower rates	39,992	(24,157)	(9,040)
Tax exempt income	(6,454)	(6,878)	(5,950)
Other, net	(1,857)	(3,625)	(2,508)
Total provision for income taxes	\$ 26,779	\$ 247,107	\$ 111,499

### Note 13: Litigation

*We are a party to lawsuits and have in the past and may in the future become a party to lawsuits involving various types of claims, including, but not limited to, unfair competition and intellectual property matters. Legal proceedings tend to be unpredictable and costly and may be affected by events outside of our control. We cannot assure you that litigation will not have an adverse effect on our financial position or results of operations.*

In November 1999, we sued Clear Logic Inc. in the United States District Court for the Northern District of California, San Jose Division, alleging that Clear Logic is unlawfully appropriating our registered mask work technology in violation of the federal mask work statute and that Clear Logic has unlawfully interfered with our relationships and contracts with our customers. The lawsuit seeks compensatory and punitive damages and an injunction to stop Clear Logic from unlawfully using our mask work technology and from interfering with our customers. Clear Logic has answered the complaint by denying that it is infringing our mask work technology and denying that it has unlawfully interfered with our relationships and contracts with our customers. Clear Logic also filed a counterclaim against us for unfair competition under California law alleging that we have made false statements to our customers regarding Clear Logic. In October 2001, the District Court ruled on summary judgment motions filed by both parties. The Court denied Clear Logic's motion for summary judgment of our claim of tortious interference with our software license, ruling that "using the bitstream [from our MAX+PLUS II software] to program a Clear Logic device violates Altera's software license." Further, the Court granted our motion for summary judgment disposing of Clear Logic's counterclaim of unfair competition. On January 4, 2002, Clear Logic filed a petition for Chapter 11 bankruptcy; as a result, all proceedings in the lawsuit have been automatically stayed. We moved to have this stay lifted, and the bankruptcy court granted our motion effective May 31, 2002. Due to the nature of the litigation with Clear Logic and because the lawsuit is still in the pre-trial stage, our management cannot estimate the total expenses that we will incur prosecuting the lawsuit. Although we cannot make any assurances as to the results of this case, we intend to pursue our claims vigorously.

In June 2000, Cypress Semiconductor Corporation sued us in the Santa Clara County Superior Court in San Jose alleging tortious interference with existing contractual relations with Right Track CAD Inc., tortious interference with economic relations, misappropriation of trade secrets, and unfair competition. In July 2000, we filed an answer that we had acquired Right Track in May 2000 and assumed the contract between Right Track and Cypress. In April 2001, Cypress added a claim based on fraud. Due to the nature of the litigation with Cypress and because the lawsuit is still in the pre-trial stage, our management cannot estimate the total expenses, the possible loss, if any, or the range of loss that may ultimately be incurred in connection with the allegations. Our management cannot ensure that Cypress will not succeed in obtaining significant monetary damages. Although we cannot make any assurances as to the results of this case, we intend to defend ourselves vigorously.

**Note 14: Segment and Geographic Information**

We operate in a single industry segment comprising of the design, development, manufacture, and sale of CMOS programmable logic integrated circuits and associated engineering development software and hardware. Our sales by major geographic area (based on destination) were as follows:

(In thousands)	Years Ended December 31,		
	2001	2000	1999
North America:			
United States	\$ 323,310	\$ 660,590	\$ 438,807
Other	53,965	126,168	30,561
Total North America	377,275	786,758	469,368
Europe	217,262	300,229	160,027
Japan	166,565	206,958	158,513
Asia Pacific	78,274	82,870	48,715
Total	\$ 839,376	\$ 1,376,815	\$ 836,623

The majority of our long-lived assets were located in the United States. Long-lived assets included property and equipment and long-term investments and other assets. Long-lived assets by country were as follows:

(In thousands)	December 31,	
	2001	2000
United States	\$ 167,506	\$ 174,361
Malaysia	25,755	13,555
Other	38,818	46,859
Total	\$ 232,079	\$ 234,775

For the years ended December 31, 2001, 2000, and 1999, no single end customer provided more than 10% of our sales.

**Note 15: Employee Benefits Plans**

We have a plan to provide retirement and incidental benefits for our eligible employees, known as the Altera Corporation Savings and Retirement Plan, or the Plan. As allowed under Section 401(k) of the Internal Revenue Code, the Plan provides tax deferred salary deductions for eligible employees. Participants in the Plan may make salary deferrals of up to 20% of the eligible annual salary, limited by the maximum dollar amount allowed by the Internal Revenue Code. For every dollar deferred under the Plan, we make a matching contribution equal to 100% up to the first 5% of the salary deferred with a maximum of \$2,000 per participant per year. Effective January 1, 2002, we accelerated the vesting of matching contributions from five to three years. This amendment applies to matching contributions made prior to January 1, 2002. Our contributions to the Plan were \$2.2 million in 2001 and \$1.3 million in both 2000 and 1999.

### ***Report of Independent Accountants***

To the Stockholders and Board of Directors of Altera Corporation:

In our opinion, the accompanying consolidated balance sheets and the related consolidated statements of operations, of stockholders' equity and of cash flows present fairly, in all material respects, the financial position of Altera Corporation and its subsidiaries at December 31, 2001 and 2000, and the results of their operations and their cash flows for each of the three years in the period ended December 31, 2001, in conformity with accounting principles generally accepted in the United States of America. These financial statements are the responsibility of the Company's management; our responsibility is to express an opinion on these financial statements based on our audits. We conducted our audits of these statements in accordance with auditing standards generally accepted in the United States of America, which require that we plan and perform the audit to obtain reasonable assurance about whether the financial statements are free of material misstatement. An audit includes examining, on a test basis, evidence supporting the amounts and disclosures in the financial statements, assessing the accounting principles used and significant estimates made by management, and evaluating the overall financial statement presentation. We believe that our audits provide a reasonable basis for our opinion.

/s/ PricewaterhouseCoopers LLP

San Jose, California  
January 18, 2002

***Supplementary Financial Data*****Quarterly Financial Information (UNAUDITED)**

(In thousands, except per share amounts)	First Quarter	Second Quarter	Third Quarter	Fourth Quarter
2001				
Net sales	\$ 287,438	\$ 215,260	\$ 174,153	\$ 162,525
Gross margin	188,243	22,542	109,632	60,260
Net income (loss)	62,992	(89,202)	20,850	(34,422)
Basic net income (loss) per share	0.16	(0.23)	0.05	(0.09)
Diluted net income (loss) per share	0.16	(0.23)	0.05	(0.09)
2000				
Net sales	\$ 272,781	\$ 340,686	\$ 395,395	\$ 367,953
Gross margin	178,191	226,001	262,701	242,928
Net income	75,154	98,262	117,989	205,502
Basic net income per share	0.19	0.25	0.30	0.52
Diluted net income per share	0.18	0.23	0.28	0.50

***Item 9. Changes in and Disagreements with Accountants on Accounting and Financial Disclosure.***

None.

## **PART III**

### ***Item 10. Directors and Executive Officers of the Registrant.***

The information concerning our executive officers required by this Item is incorporated by reference to the section in Item 1 of this Report entitled “Executive Officers of the Registrant” and the section entitled “Section 16(a) Beneficial Ownership Reporting Compliance” in our Proxy Statement. The information concerning our directors required by this Item is incorporated by reference to the section entitled “Proposal One — Election of Directors” in our Proxy Statement.

### ***Item 11. Executive Compensation.***

The sections entitled “Executive Compensation,” “Director Compensation,” and “Employment Contracts and Change of Control Arrangements” in our Proxy Statement are incorporated herein by reference.

### ***Item 12. Security Ownership of Certain Beneficial Owners and Management.***

The section entitled “Security Ownership of Certain Beneficial Owners and Management” in our Proxy Statement is incorporated herein by reference.

### ***Item 13. Certain Relationships and Related Transactions.***

The sections entitled “Director Compensation” and “Certain Relationships and Related Transactions” in our Proxy Statement are incorporated herein by reference.

## PART IV

### ***Item 14. Exhibits, Financial Statement Schedules, and Reports on Form 8-K.***

(a) The following documents are filed as part of this Report:

1. Financial Statements

The information required by this item is included in Item 8 of Part II of this Report.

2. Financial Statement Schedules.

All schedules have been omitted as they are either not required, not applicable, or the required information is included in the financial statements or notes thereto.

3. Exhibits.

<b><u>Exhibit Number</u></b>	<b><u>Exhibit</u></b>
2.1*	Assignment and Assumption Agreement dated as of November 15, 2000 between Registrant and TSMC Development, Inc.(11)
3.1	Amended and Restated Certificate of Incorporation filed with the Delaware Secretary of State on May 3, 2001.(15)
3.2	By-laws of the Registrant as adopted May 5, 1997 (which became the By-laws of the Registrant on June 19, 1997).(5)
4.1	Specimen copy of certificate for shares of common stock of the Registrant.(6)
10.1+	1987 Stock Option Plan, and forms of Incentive and Nonstatutory Stock Option Agreements, as amended March 22, 1995 and as restated effective May 10, 1995.(3)
#10.2+	1987 Employee Stock Purchase Plan, and form of Subscription Agreement, as amended and restated effective October 2001.
10.3	Form of Indemnification Agreement entered into with each of the Registrant's officers and directors.(6)
10.4+	1988 Director Stock Option Plan and form of Outside Director Nonstatutory Stock Option Agreement restated effective May 7, 1997.(9)
10.5	LSI Products Supply Agreement with Sharp Corporation, dated October 1, 1993.(1)
10.6	Letter Agreement, dated August 20, 1996, by and between Registrant and Sharp Corporation, amending the LSI Product Supply Agreement, dated October 1, 1993.(9)
10.7	Letter Agreement, dated May 22, 1997, by and between Registrant and Sharp Corporation, amending the LSI Product Supply Agreement, dated October 1, 1993.(9)
10.8	Letter Agreement, dated May 22, 1998, by and between Registrant and Sharp Corporation, amending the LSI Product Supply Agreement, dated October 1, 1993.(9)
10.9+	Altera Corporation Nonqualified Deferred Compensation Plan and Trust Agreement dated February 1, 1994 and forms of Deferred Compensation Agreement.(13)
10.10+	Addendum to Altera Corporation Nonqualified Deferred Compensation Plan and Trust and Appointment of Additional Trustee.(15)
10.11**	Wafer Supply Agreement dated June 26, 1995 between Registrant and Taiwan Semiconductor Manufacturing Co., Ltd.(2)
10.12**	Amendment No. 1 dated as of October 1, 1995 to Wafer Supply Agreement dated as of June 26, 1995 by and between Registrant and Taiwan Semiconductor Manufacturing Co., Ltd. and to Option Agreement 1 dated as of June 26, 1995 between Registrant and Taiwan Semiconductor Manufacturing Co., Ltd.(4)

10.13	Amendment of Wafer Supply Agreement dated June 1, 1997 by and between Registrant and Taiwan Semiconductor Manufacturing Co., Ltd.(9)
10.14+	1996 Stock Option Plan, as amended on May 1, 2001.(15)
#10.15+	Form of Stock Option Agreement under 1996 Stock Option Plan.
10.16	Agreement and Plan of Merger dated June 18, 1997.(5)
#10.17+	1998 Director Stock Option Plan, as amended effective October 2001.
10.18+	Form of Stock Option Agreement under 1998 Director Stock Option Plan.(15)
10.19	Product Distribution Agreement with Arrow Electronics Incorporated, effective January 26, 1999.(7)
10.20+	Form of Restricted Stock Purchase Agreement.(8)
#10.21+	Separation Agreement and General Release of Claims, dated October 19, 2001, by and between Registrant and Michael Jacobs and Letter Agreement, dated November 6, 2001, clarifying the Separation Agreement and General Release of Claims.
10.22+	2000 Non-Qualified Stock Option Plan No. 1.(10)
10.23+	Form of Stock Option Agreement for Former Employees of Northwest Logic, Inc.(10)
10.24+	Form of Stock Option Agreement for Former Founding Shareholders of Northwest Logic, Inc.(10)
10.25+	Restricted Stock Purchase Agreement between the Registrant and John Daane.(12)
10.26+	Severance Agreement, dated as of November 30, 2000, by and between John Daane and Registrant.(13)
10.27+	Change in Control Severance Agreement, dated as of November 30, 2000, by and between John Daane and Registrant.(13)
#10.28+	Letter Agreement, dated July 27, 2001, by and between Registrant and John Daane.
10.29+	Restricted Stock Purchase Agreement between the Registrant and Jordan Plofsky.(14)
#11.1	Computation of Earnings per Share (included on page 37).
#13.1	Selected Consolidated Financial Data from the Annual Report to Stockholders for the fiscal year ended December 31, 2001.
#21.1	Subsidiaries of the Registrant.
#23.1	Consent of PricewaterhouseCoopers LLP.
#24.1	Power of Attorney (included on page 52).

- (1) Incorporated by reference to the Registrant's Report on Form 10-K for the fiscal year ended December 31, 1993.
- (2) Incorporated by reference to the Registrant's Report on Form 10-Q for the quarter ended June 30, 1995.
- (3) Incorporated by reference to the Registrant's Registration Statement on Form S-8 (File No. 33-61085), as amended, which became effective July 17, 1995.
- (4) Incorporated by reference to the Registrant's Report on Form 10-K for the fiscal year ended December 31, 1995.
- (5) Incorporated by reference to the Registrant's Report on Form 10-Q for the quarter ended June 30, 1997.
- (6) Incorporated by reference to the Registrant's Report on Form 10-K for the fiscal year ended December 31, 1997.
- (7) Incorporated by reference to the Registrant's Report on Form 10-Q for the quarter ended March 31, 1999.
- (8) Incorporated by reference to the Registrant's Registration Statement on Form S-8 (File No. 333-31304), filed on February 29, 2000.
- (9) Incorporated by reference to the Registrant's Report on Form 10-K for the fiscal year ended December 31, 1999.

- (10) Incorporated by reference to the Registrant's Report on Form 10-Q for the quarter ended September 30, 2000.
- (11) Incorporated by reference to the Registrant's Report on Form 8-K, filed on December 15, 2000.
- (12) Incorporated by reference to the Registrant's Registration Statement on Form S-8 (File No. 333-54384), filed on January 26, 2001.
- (13) Incorporated by reference to the Registrant's Report on Form 10-K for the fiscal year ended December 31, 2000.
- (14) Incorporated by reference to the Registrant's Registration Statement on Form S-8 (File No. 333-56776), filed on March 9, 2001.
- (15) Incorporated by reference to the Registrant's Report on Form 10-Q for the quarter ended March 31, 2001.

# Filed herewith.

\* Confidential treatment has previously been granted for portions of this exhibit pursuant to an order of the Commission.

\*\* Confidential treatment has previously been requested for portions of this exhibit.

+ Management contract or compensatory plan or arrangement required to be filed as an exhibit to this Report on Form 10-K pursuant to Item 14(c) thereof.

(b) Reports on Form 8-K.

The following reports on Form 8-K were filed during the fourth quarter of fiscal 2001.

Current Report on Form 8-K dated October 16, 2001 and filed on October 22, 2001 announcing a ruling in the Clear Logic litigation.

## SIGNATURES

Pursuant to the requirements of Section 13 or 15(d) of the Securities Exchange Act of 1934, the Registrant has duly caused this Report on Form 10-K to be signed on its behalf, by the undersigned thereto duly authorized.

ALTERA CORPORATION

By: /s/ NATHAN SARKISIAN

Nathan Sarkisian

Senior Vice President and Chief Financial Officer

(Principal Financial and Accounting Officer)

March 5, 2002

## POWER OF ATTORNEY

Know all persons by these present, that each person whose signature appears below constitutes and appoints Nathan Sarkisian, his or her attorney-in-fact, with the power of substitution, for him or her in any and all capacities, to sign any amendments to this Report on Form 10-K, and to file the same, with exhibits thereto and other documents in connection therewith, with the Securities and Exchange Commission, hereby ratifying and confirming all that said attorney-in-fact, or his or her substitute or substitutes, may do or cause to be done by virtue hereof.

Pursuant to the requirements of the Securities Exchange Act of 1934, this Report on Form 10-K has been signed below by the following persons on behalf of the Registrant and in the capacities and on the dates indicated:

Signature	Capacity in Which Signed	Date
<u>/s/ RODNEY SMITH</u> Rodney Smith	Chairman of the Board of Directors	March 5, 2002
<u>/s/ JOHN P. DAANE</u> John P. Daane	President, Chief Executive Officer, and Director (Principal Executive Officer)	March 5, 2002
<u>/s/ NATHAN SARKISIAN</u> Nathan Sarkisian	Senior Vice President and Chief Financial Officer (Principal Financial and Accounting Officer)	March 5, 2002
<u>/s/ CHARLES M. CLOUGH</u> Charles M. Clough	Director	March 5, 2002
<u>/s/ MICHAEL A. ELLISON</u> Michael A. Ellison	Director	March 5, 2002
<u>/s/ ROBERT J. FINOCCHIO, JR.</u> Robert J. Finocchio, Jr.	Director	March 5, 2002
<u>/s/ PAUL NEWHAGEN</u> Paul Newhagen	Director	March 5, 2002

/s/ ROBERT W. REED  
Robert W. Reed

Director and Vice Chairman of the Board of Directors

March 5, 2002

/s/ DEBORAH D. RIEMAN  
Deborah D. Rieman

Director

March 5, 2002

/s/ WILLIAM E. TERRY  
William E. Terry

Director

March 5, 2002

## SUBSIDIARIES OF THE REGISTRANT

The following list identifies only Registrant's significant subsidiaries as defined in Rule 1-02(w) of Regulation S-X.

Name	Jurisdiction of Incorporation	Year Organized
Altera International, Inc.	Cayman Islands	1997
Altera International Limited	Hong Kong	1997

CONSENT OF INDEPENDENT ACCOUNTANTS

We hereby consent to the incorporation by reference in the Registration Statements on Form S-8 (No. 33-22877, No. 33-37159, No. 33-57350, No. 33-61085, No. 333-06859, No. 333-32555, No. 333-62917, No. 333-81787, No. 333-31304, No. 333-37216, No. 333-41688, No. 333-47722, No. 333-54384, No. 333-56776, and No. 333-61682) and Form S-3 (No. 333-44746) of Altera Corporation of our report dated January 18, 2002 relating to the financial statements, which appears in this Form 10-K.

/s/ PricewaterhouseCoopers LLP

PricewaterhouseCoopers LLP

San Jose, California

March 5, 2002

## Corporate Directory

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### Board of Directors

Rodney Smith  
Chairman of the Board  
Former President and Chief Executive Officer  
Altera Corporation

Robert W. Reed  
Vice Chairman of the Board  
Former Senior Vice President  
Intel Corporation

John Daane  
President and Chief Executive Officer  
Altera Corporation

Charles M. Clough  
Former Chairman, President, and Chief  
Executive Officer  
Wyle Electronics

Michael A. Ellison  
Former Chief Executive Officer  
Steller, Inc.

Robert J. Finocchio, Jr.  
Former Chairman and Chief Executive  
Officer  
Informix Corporation

Paul Newhagen  
Former Vice President, Administration  
Altera Corporation

Deborah Rieman, Ph.D.  
Former President and Chief Executive Officer  
CheckPoint Software Technologies, Inc.

William E. Terry  
Former Director and Executive Vice President  
Hewlett-Packard Company

### Corporate Officers

John Daane  
President and Chief Executive Officer

Denis Berlan  
Executive Vice President and Chief Operating  
Officer

Erik R. Cleage  
Senior Vice President, Marketing

Lance M. Lissner  
Senior Vice President, Business Development

George A. Papa  
Senior Vice President, Worldwide Sales

Jordan Plofsky  
Senior Vice President, Vertical Markets and  
Embedded Processor Products

Nathan Sarkisian  
Senior Vice President and Chief Financial  
Officer

John R. Fitzhenry  
Vice President, Human Resources

Katherine E. Schuelke  
Vice President, General Counsel and Secretary

### Appointed Officers

Misha R. Burich  
Senior Vice President, Software Development

Donald F. Faria  
Senior Vice President, Customer Marketing

John E. Turner  
Senior Vice President, Design Engineering

Bahram Ahanin  
Vice President, Design Automation

Alain Bismuth  
Vice President, Vertical Markets Strategy

Robert Blake  
Vice President, Product Planning

Melonie C. Brophy  
Vice President, Finance and Treasurer

James W. Callas  
Vice President, Finance and Corporate  
Controller

Richard Cliff  
Vice President, Design Engineering

Timothy W. Colleran  
Vice President, Component Product Marketing

Mark Dickinson  
Vice President, Excalibur Business Unit

W. Hugh Durdan  
Vice President, Technical Services

Francois Gregoire  
Vice President, Technology

Frank L. Hannig  
Vice President and Chief Information Officer

William Y. Hata  
Vice President, Product Engineering

Ben A. Lee  
Vice President, Asia Pacific

Craig Lytle  
Vice President, Intellectual Property Business  
Unit

Alan H. Markow  
Vice President, Corporate Marketing

Thomas B. Murchie  
Vice President, Operations

Chris T. K. Oh  
Vice President, Asia Pacific Operations

Timothy J. Propeck  
Vice President, North America Sales

Timothy J. Southgate  
Vice President, Software and Tools Marketing

Nigel Toon  
Vice President and Managing Director, Europe

Scott Wylie  
Vice President, Investor Relations

### Corporate Headquarters

101 Innovation Drive  
San Jose, California 95134  
(408) 544-7000

### Independent Accountants

PricewaterhouseCoopers LLP  
San Jose, California

### Registrar/Transfer Agent

EquiServe Trust Company  
P.O. Box 43010  
Providence, Rhode Island 02940  
(781) 575-3120  
<http://www.EquiServe.com>

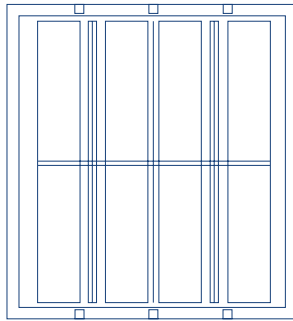
### Web Site

For current information on Altera  
Corporation, visit our worldwide web site at  
<http://www.altera.com>.

### Additional Information

Please direct all requests to:

Investor Relations  
101 Innovation Drive  
San Jose, California 95134  
(408) 544-7707



101 Innovation Drive • San Jose, CA 95134 • Telephone (408) 544-7000  
<http://www.altera.com>