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11 UNITED STATES DISTRICT COURT
12 NORTHERN DISTRICT OF CALIFORNIA
13
14 SAN JOSE DIVISION

15 HYNIX SEMICONDUCTOR INC.,
16 HYNIX SEMICONDUCTOR AMERICA
17 INC., HYNIX SEMICONDUCTOR U.K.
18 LTD., and HYNIX SEMICONDUCTOR
19 DEUTSCHLAND GmbH,

18 Plaintiffs,

19 vs.

20 RAMBUS INC.,

21 Defendant.

CASE NO. CV 00-20905 RMW

**RAMBUS'S NOTICE OF MOTION AND
MOTION FOR SUMMARY JUDGMENT
OF INFRINGEMENT; CORRECTED
MEMORANDUM OF POINTS AND
AUTHORITIES IN SUPPORT THEREOF**

**[Declarations of Peter A. Detre and Robert J.
Murphy Filed Separately]**

**Date: March 23, 2004
Time: 9:00 a.m.
Ctrm: 6 (Hon. Ronald M. Whyte)**

**ORIGINAL
FILED**

JAN 27 2004

**RICHARD W. WIEKING
CLERK, U.S. DISTRICT COURT
NORTHERN DISTRICT OF CALIFORNIA**

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1 MEMORANDUM OF POINTS AND AUTHORITIES

2 **I. INTRODUCTION**

3 Over 12 years ago, Michael Farnwald and Mark Horowitz, both professors of
4 electrical engineering, filed a patent application teeming with new ideas for increasing the speed
5 and efficiency of memory devices. Drs. Farnwald and Horowitz were convinced that, as the
6 speeds of computer processors continued to increase exponentially, their ideas would have to be
7 used if memory devices were to keep up and a data flow bottleneck avoided. It is now clear that
8 Drs. Farnwald and Horowitz were correct in their predictions. All of the Rambus patents
9 asserted in this case stem from that original application filed by Drs. Farnwald and Horowitz, and
10 the accused memory devices in this case, sold primarily for use in the main memory of
11 computers, are able to achieve the performance that the marketplace demands only through use of
12 a number of the inventions claimed in those patents.

13 As set forth below, Hynix's infringement of Rambus's patents is made clear by
14 Hynix's own documents describing the design and operation of their SDRAM and DDR SDRAM
15 devices. Therefore, Rambus respectfully requests that the Court grant summary judgment of
16 infringement with respect to the following asserted claims.

17 U.S. Patent No. 5,953,263, claims 1, 2, 3, 4;

18 U.S. Patent No. 6,038,195, claims 11, 17, 18, 19;

19 U.S. Patent No. 6,034,918, claims 18, 24, 33;

20 U.S. Patent No. 6,324,120, claims 1, 5, 6, 7, 12, 26, 28, 30, 33, 34, 38;

21 U.S. Patent No. 6,452,863, claims 14, 15, 16;

22 U.S. Patent No. 6,426,916, claims 1, 3, 9, 12, 14, 26, 28, 31, 37, 40; and

23 U.S. Patent No. 6,378,020, claims 31, 32, 35, 36, 38.¹

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27 ¹ The claims are asserted against both SDRAM and DDR SDRAM devices, except for claim 19 of
28 the '195 patent, claim 33 of the '918 patent, claims 5, 28 and 38 of the '120 patent, claims 3, 31
and 40 of the '916 patent, and the claims of the '020 patent, which are asserted only against DDR
SDRAMs.

1 **II. BACKGROUND**

2 **A. Rambus's Inventions**

3 As discussed in Rambus's Opening Claim Construction Brief, the patents at issue
4 in this case all stem from an original application filed on April 18, 1990 and contain substantially
5 identical written descriptions. In the original application, the inventors, Drs. Farmwald and
6 Horowitz, described a comprehensive solution for improving the speed and efficiency of memory
7 devices that was comprised of multiple individual inventions. The claims that are the subject of
8 this motion focus on certain of those inventions.²

9 Certain asserted claims, for example, involve storage of a value representative of a
10 delay time in a register on a synchronous semiconductor memory device, while others involve the
11 sending of "block size information" to a synchronous memory device so that the device can
12 respond to a read request with a variable amount of data depending on the value of the block size
13 information. These two aspects of the asserted claims are described in Rambus's Opening Claim
14 Construction Brief. CC Brief at 5-6. Some other key features of Rambus's inventions for
15 purposes of this motion are described below.

16 **1. Precharge Information**

17 As discussed in Rambus's Opening Claim Construction Brief, "sense amplifiers"
18 are used in DRAMs to detect and amplify the small voltage differences representing the
19 information stored in memory cells, before those values are transferred to the input/output pins of
20 the DRAM. CC Brief at 3, n.3. These sense amplifiers must be set to a pre-defined voltage state
21 -- "precharged" -- so that they will be able properly to differentiate between high and low voltages
22 stored in the memory cells. *Id.* at 18-19.

23 In some circumstances, however, it may not be efficient to precharge the sense
24 amplifiers immediately after a read operation. As previously discussed, DRAMs are organized
25 in arrays of rows and columns of memory cells. CC Brief at 2-3. When data is read from
26 DRAMs, an entire row of cells is activated (i.e. the data from each cell in that row is transferred

27 ² General technical background relating to DRAMs, the category of memory devices that include
28 Hynix's accused devices, can be found in Rambus's Opening Claim Construction Brief.
Rambus's Opening Claim Construction Brief ("CC Brief") at 1-4.

1 to the sense amplifiers) and then the data from the desired column(s) within that row are
2 transferred to the data pins. It would be inefficient to precharge the sense amplifiers in a situation
3 where the next read operation is to be from the same row since it would have to be precharged
4 and then activated again unnecessarily, thus adding further delay and unnecessary power
5 consumption.

6 Certain of the asserted Rambus patent claims involve sending precharge
7 information to the memory device in conjunction with a read command. *See, e.g.,* '120 patent,
8 claim 33 (Section III.C.4.d, *infra*). This precharge information could, for example, instruct the
9 memory device to precharge the sense amplifiers at the conclusion of the read operation.

10 **2. Dual Edge Clocking**

11 Certain asserted claims involve increasing the rate of data transfer to or from the
12 memory device by transferring two bits of data per data pin per clock cycle, instead of just one bit
13 as in traditional systems. This is accomplished by transferring one bit in response to the rising
14 edge of the clock (when the clock signal transitions from a low to a high voltage) and one bit in
15 response to the falling edge (when the clock signal transitions from a high to a low voltage). *See,*
16 *e.g.,* '120 patent, claim 33 (Section III.C.4.d, *infra*).

17 **3. On-chip DLL**

18 A delay locked loop or DLL is, as the parties have agreed, circuitry “including a
19 variable delay line, that uses feedback to adjust the amount of delay of the variable delay and to
20 generate a signal having a controlled timing relationship with another signal.” Joint Claim
21 Construction and Prehearing Statement (“JCCS”) at 3. Certain asserted claims involve a DLL on
22 a memory device that uses an external clock signal to generate an internal clock signal and then
23 outputs data synchronously with respect to the internal clock signal – that is, the DLL uses
24 feedback to adjust its variable delay and to generate an internal clock signal having a controlled
25 relationship with the external clock signal. *See, e.g.,* '918 patent, claim 33 (Section III.C.3.c,
26 *infra*).

27 One use of this invention involves using the DLL to adjust the internal clock that
28 times the output of data so that the output data is aligned with the external clock. At high data

1 speeds the increased precision of the synchronization provided by the DLL between the timing of
2 data output and the timing of the system (dictated by the external clock signal) is important to
3 ensure that the controller is able to read the data during the window of time that the data is valid.

4 **B. The Accused Products**

5 Hynix's SDRAM and DDR SDRAM devices are memory devices that store
6 information in memory cells. Information is written to or read from the memory device by a
7 "controller" which can be a CPU in a computer system or a specialized memory controller
8 connected to the memory device (and, potentially, other memory devices) via a set of signal lines
9 known as a "bus." Hynix's devices are *synchronous* memory devices in the sense that address,
10 input data and control signals are recognized, and output data signals are transferred, in response
11 to an external clock.

12 **1. Features of Hynix's SDRAMs and DDR SDRAMs**

13 Each Hynix SDRAM and DDR SDRAM contains a "mode register" that stores
14 various parameters relating to the operation of the device. *See* Declaration of Robert J. Murphy
15 in Support of Rambus's Motion for Summary Judgment ("Murphy Decl.") ¶ 8. During an
16 initialization sequence, a "mode register set" command is issued and data to be stored in the mode
17 register is transmitted from the controller to the DRAM via the bus lines used for address
18 information during read and write operations. *Id.* ¶¶ 8, 23.

19 One of the values stored in the mode register in both SDRAMs and DDR
20 SDRAMs represents what is known as the "CAS latency." *Id.* ¶ 9. As in Rambus's claims, the
21 CAS latency is a value representative of a delay time after which the SDRAM or DDR SDRAM
22 responds to a read request.

23 Another value stored in the mode register in both SDRAMs and DDR SDRAMs is
24 called the "burst length." *Id.* ¶ 44. Like the "block size information" described in Rambus's
25 patents, the "burst length" signifies the amount of data to be transferred in response to a read or
26 write request.

27 Both SDRAMs and DDR SDRAMs include an "autoprecharge" feature that
28 involves sending precharge information to the DRAM in conjunction with read and write

1 commands as in Rambus's patents. *Id.* ¶ 75. When the read or write command is issued "with
2 autoprecharge," the sense amplifiers in the memory bank that is active during the read or write
3 operation will be precharged as a part of that read or write cycle without the need of an additional
4 "precharge" command separate from the read or write command.

5 **2. Additional Features of Hynix's DDR SDRAMs**

6 Hynix's DDR SDRAM devices differ from its SDRAM devices in a number of
7 respects, however only two features of DDR SDRAMs that are not in SDRAMs are relevant here:
8 dual-edge clocking and on-chip delay locked loop.

9 First, unlike SDRAMs which use only the rising edges of the clock signal to time
10 data input and output, DDR SDRAMs use both the rising and falling edges as in Rambus's
11 patents. *Id.* ¶¶ 68-69. By transferring two bits of data per pin during each clock cycle in this
12 way, DDR SDRAMs double the rate of data flow (hence "DDR" or "double data rate").

13 Second, Hynix's DDR SDRAMs contain a "delay locked loop" or "DLL" as in
14 Rambus's patents. *Id.* ¶¶ 38-39. In Hynix's DDR SDRAMs, the DLL generates an internal clock
15 signal, designated as "CLK_DLL" that is synchronized with the system clock and that the DRAM
16 uses to time the output of data.

17 **3. Representative Products**

18 Hynix has designated one SDRAM product and one DDR SDRAM product as
19 representative of their SDRAM and DDR SDRAM offerings generally for purposes of the
20 patents-in-suit.³ Declaration of Peter A. Detre in Support of Rambus's Motion for Summary
21 Judgment ("Detre Decl.") ¶ 2 & Ex. A. Thus, this motion focuses on those representative
22 products: Hynix's SDRAM with part number HY57V28820AT and Hynix's DDR SDRAM with
23 part number HY5DU2822T. *Id.* Hynix's data sheets for the representative products are attached
24 to the Declaration of Peter A. Detre filed herewith as Exhibits B and C and will be referred to
25 hereafter as "SDRAM Data Sheet" and "DDR Data Sheet," respectively; in addition, a general

26
27 ³ While Hynix's designation of representative products was in connection with the patents-in-suit
28 at the time which did not include the patents later added by Rambus by amendment, the asserted
claims of those later-added patents are alleged to be infringed by the same features of Hynix's
products as the earlier asserted patents.

1 data sheet regarding “Hynix SDRAM Device Operation” is attached as Exhibit D and will be
2 referred to hereafter as “SDRAM Operation.”

3 **III. ARGUMENT**

4 **A. Legal Standard**

5 Summary judgment should be granted when there is no genuine issue of material
6 fact and the moving party is entitled to judgment as a matter of law. Fed. R. Civ. P. 56(c);
7 *Celotex Corp. v. Catrett*, 477 U.S. 317, 322 (1986). Although the Court must view the evidence
8 in the light most favorable to the non-movant, in order to establish that there is a “genuine” issue
9 as to an essential element of its case, the non-movant “must do more than merely raise some
10 doubt as to the existence of a fact; evidence must be forthcoming from the non-movant which
11 would be sufficient to require submission to the jury of the dispute over the fact.” *Avia Group*
12 *Int’l, Inc. v. L.A. Gear California*, 853 F.2d 1557, 1560 (Fed. Cir. 1988) (citing *Anderson v.*
13 *Liberty Lobby, Inc.*, 477 U.S. 242, 248 (1986)).

14 Whether an accused device infringes a patent is determined through a two-step
15 process. *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 999 (Fed. Cir. 1995 (en banc),
16 *aff’d*, 116 S. Ct. 1384 (1996). First, the Court interprets the claim language as a matter of law.
17 *Id.* at 970-71, 976. Second, the Court applies the claim to the accused device. *Id.* at 976. Here,
18 under the appropriate construction of the claim language, it is clear that Hynix’s memory devices
19 contain each and every element of the claims that are the subject of this motion.⁴

20 **B. Claim Limitations**

21 Many of the limitations in Rambus’s asserted claims appear in various different
22 claims. In order to streamline the argument, Rambus here shows that Hynix’s accused devices
23 meet certain of these limitations prior to discussing specific claims that the accused devices
24

25 _____
26 ⁴ In addition to directly infringing Rambus’s claims by making, using, offering to sell, selling, and
27 importing into the United States its SDRAMs and DDR SDRAMs, 35 U.S.C. § 271(a), Hynix is
28 also liable for actively inducing the infringement of Rambus’s patents by its customers who
operate the devices as shown in Hynix’s documentation, 35 U.S.C. § 271(b), and for contributing
to the infringement of Rambus’s patents by its customers who incorporate Hynix’s devices into
computer systems or other products, 35 U.S.C. § 271(c).

1 infringe. The limitations have been grouped according to the aspect of Rambus's inventions to
2 which they relate.

3 **1. General**

4 **a. Synchronous semiconductor memory device**⁵

5 Hynix's SDRAMs and DDR SDRAMs are synchronous semiconductor devices.
6 See Murphy Decl. ¶¶ 5-6. Indeed, "SDRAM" stands for "*Synchronous* DRAM" and "DDR
7 SDRAM" stands for "Double Data Rate *Synchronous* DRAM." Rambus has proposed that
8 "synchronous memory device" be construed as "a memory device in which address, input data,
9 and control signals are recognized and output data signals are transferred in response to an
10 external clock." Hynix's SDRAMs meet this definition because "all inputs and outputs [are]
11 referenced to [the] positive edge of the system clock." SDRAM Data Sheet at 1. Hynix's DDR
12 SDRAMs meet this definition because "all addresses and control inputs are latched on the rising
13 edges of the CK [external clock]" and "data transitions are aligned with CK." DDR Data Sheet at
14 3. Hynix's proposed construction of "synchronous memory device" is broader than Rambus's and
15 includes all "memory devices in which an external clock is used for timing purposes." Therefore
16 Hynix's SDRAMs and DDR SDRAMs are synchronous memory devices under either party's
17 proposed construction.

18 **b. Memory section which includes a plurality of memory cells**⁶

19 Hynix's SDRAMs and DDR SDRAMs have at least one memory section which
20 includes a plurality of memory cells. See Murphy Decl., ¶ 7. In fact, Hynix's SDRAMs and
21 DDR SDRAMs each have four memory banks which constitute memory sections and, in the 128
22 Mb density, each of these banks contains "8M x 4" or approximately 32 million cells to store
23 approximately 32 million bits of information. SDRAM Data Sheet at 1; DDR SDRAM Data
24 Sheet at 7.

25
26
27 ⁵ See, e.g., '263, claim 1 (Section C.1.a., *infra*).

28 ⁶ See, e.g., '263 patent, claim 1 (Section C.1.a, *infra*).

1 c. **Clock receiver circuitry to receive an external clock signal**⁷

2 Hynix SDRAMs and DDR SDRAMs contain clock receiver circuitry to receive an
3 external clock signal. *See* Murphy Decl., ¶ 26. Such an external clock signal is shown, for
4 example, at pin 38 (“CLK”) of the Hynix SDRAM Data Sheet and at pin 45 (“CK”) of the Hynix
5 DDR Data Sheet.

6 d. **Receiving a read request or an operation code specifying a read**
7 **operation from the bus controller**⁸

8 Hynix’s SDRAMs and DDR SDRAMs receive read requests from the bus
9 controller, such as a CPU or a specialized memory controller. *See* Murphy Decl. ¶ 15. The
10 combination of signals that will signify a “read request” is shown in the “truth tables” in the
11 Hynix data sheets. Both SDRAMs and DDR SDRAMs can receive two types of read requests:
12 “read” and “read with autoprecharge.” A “read” is specified by /CS low, /RAS high, /CAS low,
13 /WE high, and A10 low; a “read with autoprecharge is specified by the same combination of
14 signals, except that A10 is high instead of low.

15 The combination of the first four signals above, which are identical for a “read”
16 and a “read with autoprecharge,” indicate that a read operation of one or the other type is to be
17 performed. Therefore, this combination of signals along with either state of the A10 bit constitute
18 “operation codes” specifying a read operation. Rambus has proposed that “operation code” be
19 construed as “one or more bits to specify a type of action.” The five bits, identified above, that
20 specify a read operation plainly meet this definition. Hynix’s proposed construction – “bits in a
21 field within a packet or computer code instruction that identifies what type of action to be
22 performed” – appears to have been jury-rigged precisely to exclude the manner in which
23 operations are transmitted to Hynix’s devices and should be rejected.

24
25
26
27 ⁷ *See, e.g.*, ’195 patent, claim 11 (Section C.2.a., *infra*).

28 ⁸ *See, e.g.*, ’918 patent, claim 18 (Section C.3.a, *infra*).

1 e. A plurality of input receivers to sample the read request or the
2 operation code specifying a read operation synchronously with
3 respect to the external clock signal⁹

4 As noted above, a read request or operation code is transmitted to the SDRAM or
5 DDR SDRAM using five signals each of which is received at a different pin by the DRAM. Each
6 pin has its own associated input receiver. Moreover, the signals making up the read request are
7 sampled synchronously with respect to the external clock signal since all inputs to Hynix's
8 SDRAMs and DDR SDRAMs, including control signals, are sampled synchronously with respect
9 to the external clock signal. See Murphy Decl. ¶¶ 63, 89.

10 f. Input receiver circuitry to receive address information
11 synchronously with respect to the external clock signal¹⁰

12 Hynix's SDRAMs and DDR SDRAMs receive address information at the address
13 pins: A0 to A11.¹¹ SDRAM Data Sheet at 2; DDR Data Sheet at 4. The address information is
14 received synchronously with respect to the external clock signal along with the other inputs to the
15 devices. See Murphy Decl. ¶ 142.

16 g. Output drivers, coupled to an external bus, to output data on
17 the bus in response to a read request or an operation code
18 specifying a read operation¹²

19 Hynix's SDRAMs and DDR SDRAMs contain output drivers to output data via
20 data pins onto an external bus. See Murphy Decl. ¶ 14. The output drivers are contained in the
21 "I/O Buffer & Logic" shown in the SDRAM block diagram and the "Output Buffer" shown in the
22 DDR SDRAM block diagrams. SDRAM Data Sheet at 3; DDR Data Sheet at 7-9. These drivers
23 are connected to the data pins, which, in turn are to be connected to an external bus. *Id.*; see
24 Murphy Decl. ¶ 14.

25 ⁹ See, e.g., '120 patent, claim 30 (Section C.4.c, *infra*).

26 ¹⁰ See, e.g., '020 patent, claim 32 (Section C.7.c, *infra*).

27 ¹¹ Hynix's SDRAM and DDR SDRAM devices contain more rows than columns. Therefore,
28 while all 12 address pins are used to transmit the row address, only the first 10 (A0 to A9) are
used to transmit the column address at the time of a read command (leaving A10 free to provide
precharge information).

¹² See, e.g., '263 patent, claim 2 (Section C.1.b, *infra*).

1 **h. Output data synchronously with respect to the external clock**¹³

2 Hynix’s SDRAM and DDR SDRAM devices output data synchronously with
3 respect to an external clock. *See* Murphy Decl. ¶ 16. In the case of SDRAMs, “[a]ll . . . outputs
4 are referenced to [the] positive edge of [the] system clock.” SDRAM Data Sheet at 1. In the case
5 of DDR SDRAMs, the delay locked loop on the chip, discussed further below, ensures that “data
6 transitions are aligned with CK [the external clock].” DDR Data Sheet at 3.

7 **2. Programmable Latency**

8 **a. Programmable register**¹⁴

9 The parties agree that a “programmable register” is “a register whose contents can
10 be modified based on information received from outside the device containing the register.” Each
11 Hynix SDRAM and DDR SDRAM device contains a “mode register.” SDRAM Operation at 1,
12 15; DDR Data Sheet at 20. The contents of the mode register can be modified through a “mode
13 register set” command. *Id.* When that command is invoked, information transmitted to the
14 device from outside the device is written to the mode register. Thus, the mode register is a
15 programmable register. *See* Murphy Decl. ¶ 8.

16 **b. A value (delay time code) representative of a delay time**
17 **(number of clock cycles of the external clock) after which the**
18 **memory device responds to a read request (to transpire before**
19 **data is output onto the bus after receipt of a read request)**¹⁵

20 One of the values stored in the mode register is the “read latency” or “CAS
21 latency” of the device. In SDRAMs, “[t]he first data is available after /CAS latency number of
22 clock cycles” measured from the read command. SDRAM Operation at 2. In DDR SDRAMs,
23 the CAS latency “is the delay, in clock cycles, between the registration of a Read command and
24 the availability of the first burst of output data.”¹⁶ Thus, after this “delay” has expired, the device
25 responds to the read command by making the output data available.

26 Rambus has proposed that “delay time” be construed as “an amount of time before

27 ¹³ *See, e.g.*, ’263 patent, claim 2 (Section C.1.b, *infra*).

28 ¹⁴ *See, e.g.*, ’263 patent, claim 1 (Section C.1.a, *infra*).

¹⁵ *See, e.g.*, ’263 patent, claim 1 (Section C.1.a, *infra*).

¹⁶ There is a subtle difference in the timing of data output between Hynix’s SDRAMs and DDR SDRAMs that is not material to the question of infringement. *See* Murphy Decl. ¶ 9 & n. 1.

1 commencing a subsequent action.” Under Rambus’s construction, the CAS latency value in
2 Hynix’s devices is representative of a “delay time” after which the device responds to a read
3 request. Hynix has proposed that “delay time” be construed as “the time between the initiation of
4 a memory access and the availability of data at the outputs.” While Rambus has argued that
5 Hynix’s proposed construction is ambiguous and unnecessarily specific, the registration of a read
6 command is at least one reasonable time to refer to as the “initiation of a memory access.” The
7 value representing the CAS latency stored in the mode register is, therefore, a value
8 representative of delay time within the meaning of Rambus’s patent claims under either party’s
9 construction of “delay time.” *See* Murphy Decl. ¶¶ 9-11. Moreover, this value stored in the
10 mode register of Hynix’s devices, as the quotes above indicate, represents a number of cycles of
11 the external clock.

12 **c. Initialization sequence during which the programmable register**
13 **stores the value after power is applied to the device**¹⁷

14 Both Hynix SDRAMs and DDR SDRAMs store the value representing the CAS
15 latency in the mode register via a “mode register set” command during an initialization sequence.
16 *See* Murphy Decl. ¶¶ 22-23; SDRAM Operation at 1 (“SDRAM must be initialized with the
17 proper power-up sequence to the following . . . 5. Issue a mode register set command to initialize
18 the mode register.”); DDR Data Sheet at 18 (“DDR SDRAMs must be powered up and initialized
19 in a predefined manner. . . . [A] MODE REGISTER SET command should be issued for the
20 Mode Register . . . to program the operating parameters.”).¹⁸

21 The initialization sequence for Hynix SDRAMs and DDR SDRAMs makes clear
22 that the mode register set command, which stores the value specifying the CAS latency in the
23 mode register, follows power being supplied to the device. *See* Murphy Decl. ¶ 35. Thus,
24 Hynix’s SDRAM Operation lists as step 1 of the initialization sequence “Apply power,” and as
25 step 5, “Issue a mode register set command to initialize the mode register.” SDRAM Operation at
26 1. Likewise, Hynix’s DDR Data Sheet describes applying power to the DDR SDRAMs during

27 ¹⁷ *See, e.g.*, ’263 patent, claim 4 (Section C.1.d, *infra*).

28 ¹⁸ A mode register set command may be issued after initialization to change the parameters, but
must be issued to initialize the device. SDRAM Operation at 1.

1 the “power-up sequence and device initialization” prior to issuing a mode register set command.
2 DDR Data Sheet at 18.

3 **d. Value is stored in the register in response to an operation code**¹⁹

4 As noted above, the CAS latency is stored in the mode register in Hynix’s
5 SDRAMs and DDR SDRAMs in response to a mode register set command. This mode register
6 set command is specified by a combination of signals sent to the DRAMs (namely, /RAS, /CAS,
7 CS, and /WE all low). SDRAM Operation at 1. Thus, the mode register set command is
8 conveyed to the DRAMs via an “operation code” – one of more bits to specify a type of action –
9 according to Rambus’s proposed construction of the term. See Murphy Decl. ¶ 79.

10 **3. Variable block size**

11 **a. Receiving block size information from a bus controller, wherein**
12 **the block size information defines an amount of data to be**
13 **output (input) by the memory device onto a bus in response to a**
14 **read request or an operation code specifying a read operation**
15 **(write operation)**²⁰

16 Hynix’s SDRAM and DDR SDRAM devices receive block size information
17 defining an amount of data to be output by the memory device in response to a read request or
18 input by the memory device in response to a write request from a controller. See Murphy Decl.
19 ¶¶ 44-46. During a mode register set operation, the controller provides a “burst length” value that
20 is stored in the mode register. SDRAM Operation at 15; DDR Data Sheet at 20, 21. The burst
21 length specifies the number of bits of data to be read from or written to the memory device during
22 a read or write operation, respectively. SDRAM Operation at 2; DDR Data Sheet at 21. This
23 burst length value satisfies both Rambus’s and Hynix’s proposed construction of “block size
24 information.”

25 Rambus has proposed that “block size information” be construed as “a value
26 representative of a quantity of data to be transferred during a memory read or write operation.”
27 Clearly, the burst length stored in the mode register in Hynix’s SDRAMs and DDR SDRAMs
28 meets this definition since it equals the number of bits of data to be transferred during a memory

¹⁹ See, e.g., ’916 patent, claim 28 (Section C.6.b, *infra*).

²⁰ See, e.g., ’918 patent, claim 18 (Section C.3.a, *infra*).

1 read or write operation from each pin. (Therefore, it is representative of the quantity of data to be
2 transferred from each pin; it is also representative of the quantity of data to be transferred from
3 the memory device, since this quantity can be obtained by multiplying the burst length by the
4 number of data pins; it is also representative of the quantity of data to be transferred from the
5 memory system, since this quantity can be obtained by multiplying the quantity of data to be
6 transferred from each memory device by the number of devices).

7 Hynix proposes that “block size information” be construed as “information that
8 specifies the total amount of data that is to be transferred on the bus in response to a [transaction]
9 request.” While, as Rambus has previously argued, Hynix’s proposed construction is not as clear
10 as Rambus’s, under the most natural reading, the burst length value stored in the mode register
11 would qualify as block size information. As noted above, the block size information does specify
12 the total amount of data to be transferred on the bus from a memory device in response to a
13 transaction request because that quantity can be obtained by multiplying the burst length by the
14 number of data pins.

15 **b. Input receiver circuitry, including a plurality of input receivers,**
16 **to sample the block size information synchronously with respect**
to the external clock signal²¹

17 The block size information (burst length) is received via three pins, A0, A1 and
18 A2, SDRAM Operation at 15; DDR Data Sheet at 20, each with an associated input receiver.
19 Murphy Decl. ¶ 83. The block size information, like the other information written to the mode
20 register, is sampled synchronously with respect to the external clock. SDRAM Data Sheet at 1
21 (“All inputs . . . referenced to positive edge of system clock.”); DDR Data Sheet at 3 (“All . . .
22 control inputs . . . latched on rising edges of the clock.”).

23 **4. Precharge Information**

24 **a. Operation code specifying a read operation includes precharge**
25 **information**²²

26 Both Hynix SDRAMs and DDR SDRAMs include precharge information in read
27 commands. See Murphy Decl. ¶ 75. As the SDRAM and DDR SDRAM “Command Truth

28 ²¹ See, e.g., ’120 patent, claim 26 (Section C.4.a, *infra*).

²² See, e.g., ’120 patent, claim 33 (Section C.4.d, *infra*).

1 Tables” makes clear, a read command can be with or without “autoprecharge” depending on the
2 state of the A10 bit. SDRAM Data Sheet at 12; DDR Data Sheet at 10. If the read is “with
3 autoprecharge,” the sense amplifiers in the memory bank from which the data is read will be
4 precharged as a part of the read cycle. SDRAM Operation at 7. Thus, the state of the A10 bit in a
5 read command constitutes precharge information, since it instructs the memory device whether to
6 perform a precharge operation as a part of the read cycle.

7 **5. DDR**

- 8 a. **First portion of output data is output synchronously with**
9 **respect to (in response to) a rising edge transition of the**
10 **external clock signal and a second portion of the amount of**
11 **data is output synchronously with respect to (in response to) a**
12 **falling edge transition of the external clock signal**²³

13 In Hynix’s DDR SDRAM devices, “DDR” stands for “double data rate” precisely
14 because transferring data on both rising and falling edges of the clock signal allows two data bits
15 to be transferred per clock cycle (per pin) as opposed to one bit as in SDRAMs. Hynix’s DDR
16 Data Sheet makes clear that output data is aligned with both rising and falling edge transitions of
17 the clock. DDR Data Sheet at 3. In the example of a burst length of 4 shown in the timing
18 diagram on page 24 of the DDR Data Sheet, data bits A0 and A2 are output on rising edge
19 transitions of the clock (CLK), while A1 and A3 are output on falling edge transitions. *See*
20 *Murphy Decl.* ¶¶ 68-69.

21 **6. DLL**

- 22 a. **A delay locked loop, coupled to the clock receiver circuitry, to**
23 **generate an internal clock signal using at least the external**
24 **clock signal wherein data is output onto the bus synchronously**
25 **with respect to the at least one internal clock signal**²⁴

26 The parties agree that a “delay locked loop” is “circuitry on the device, including a
27 variable delay line, that uses feedback to adjust the amount of delay of the variable delay line and
28 to generate a signal having a controlled timing relationship relative to another signal.” Hynix’s
29 DDR SDRAMs contains a DLL, or delay locked loop, as shown, for example, in the block
30 diagrams on pages 7-9 of the DDR Data Sheet. The DLL receives the external clock (CLK) as an

²³ *See, e.g.,* ’020 patent, claim 30 (Section C.7.a, *infra*).

²⁴ *See, e.g.,* ’195 patent, claim 19 (Section C.2.d, *infra*).

1 input and generates an internal clock (CLK_DLL). This internal clock signal is then supplied to
2 the output buffer. The purpose of the DLL is to align the output data and the external clock.
3 DDR Data Sheet at 3. It follows that all of the limitations of claim 19 of the '195 patent are
4 satisfied by Hynix DDR SDRAMs:

5 The devices contain a delay locked loop (DLL) to generate an internal clock signal
6 (CLK_DLL) using the external clock signal (CLK), and the delay locked loop must be coupled to
7 the clock receiver circuitry in order to receive the external clock signal. Moreover, the point of
8 generating the internal clock signal is to supply that signal to the output drivers so that they will
9 output data in response to that signal which has been adjusted by the DLL so that data is aligned
10 with the external clock. *See* Murphy Decl. ¶¶ 39-40.

11 **C. Patent Claims**

12 The claims that are the subject of this motion are discussed below with reference
13 to the claim elements analyzed above. The patents themselves are attached to prior pleadings in
14 this matter.²⁵

15 **1. U.S. Patent No. 5,953,263**

16 **a. Claim 1**

17 Claim 1 of the '263 patent claims:

18 A synchronous semiconductor memory device having at
19 least one memory section which includes a plurality of memory
20 cells, the memory device comprises:

21 a programmable register to store a value which is
22 representative of a delay time after which the memory device
23 responds to a read request.

24 Hynix's SDRAMs and DDR SDRAMs contain each of the limitations of claim 1.

25 *See* Sections B.1.a, b, B.2.a, b.

26 **b. Claim 2**

27 Claim 2 of the '263 patent claims "[t]he synchronous memory device of claim 1,

28 ²⁵ Listing them in the order in which they appear in this brief, the patents can be found as the following exhibits to prior pleadings: The '263, '195 and '918 patents are attached as exhibits B, I, and G, respectively, to Hynix's original Complaint, filed on August 29, 2000; The '120, '863, '916, and '020 patents are attached as exhibits A, D, C and B, respectively, to Rambus's Second Amended Complaint and Amended Counterclaim, filed on November 25, 2002.

1 further including output drivers, coupled to an external bus, to output data on the bus, in response
2 to the read request, synchronously with respect to an external clock.”

3 Hynix’s SDRAMs and DDR SDRAMs contain each of the additional limitations
4 of claim 2. *See* Sections B.1.g, h.

5 **c. Claim 3**

6 Claim 3 of the ’263 patent claims “[t]he synchronous memory device of claim 2
7 wherein the value is representative of a number of clock cycles of the external clock.”

8 Hynix’s SDRAMs and DDR SDRAMs contain the additional limitation of claim 3.
9 *See* Section B.2.b.

10 **d. Claim 4**

11 Claim 4 of the ’263 patent claims “[t]he synchronous memory device of claim 1
12 wherein, during an initialization sequence, the programmable register stores the value.”

13 Hynix’s SDRAMs and DDR SDRAMs contain the additional limitation of claim 4.
14 *See* Section B.2.c.

15 **2. U.S. Patent No. 6,038,195**

16 **a. Claim 11**

17 Claim 11 of the ’195 patent claims:

18 A synchronous semiconductor memory device having at
19 least one memory section including a plurality of memory cells, the
memory device comprising:

20 clock receiver circuitry to receive an external clock signal;

21 at least one register to store a value which is representative
22 of a delay time; and

23 wherein in response to a read request, the memory device
24 outputs data after the delay time transpires and synchronously with
respect to the external clock signal.

25 Hynix’s SDRAMs and DDR SDRAMs contain each of the limitations of claim 11.
26 *See* Sections B.1.a, b, c, h, B.2.a, b.

27 **b. Claim 17**

28 Claim 17 of the ’195 patent claims “[t]he synchronous memory device of claim 11

1 where the value is representative of a number of clock cycles of the external clock signal.”

2 Hynix’s SDRAMs and DDR SDRAMs meet the additional limitation of claim 17.

3 See Section B.2.b.

4 **c. Claim 18**

5 Claim 18 of the ’195 patent claims “[t]he memory device of claim 17 wherein the
6 value which is representative of the delay time is stored in the register after power is supplied to
7 the device.”

8 Hynix’s SDRAMs and DDR SDRAMs meet the additional limitation of claim 18.

9 See Section B.2.c.

10 **d. Claim 19**

11 Claim 19 of the ’195 patent claims:

12 The memory device of claim 17 further including:

13 a delay locked loop, coupled to the clock receiver circuitry,
14 to generate an internal clock signal using at least the external clock
signal; and

15 wherein the plurality of output drivers output data in
16 response to the internal clock signal.

17 Hynix’s DDR SDRAMs meet the additional limitation of claim 19. See Section

18 B.6.a.

19 **3. U.S. Patent No. 6,034,918**

20 **a. Claim 18**

21 Claim 18 of the ’918 patent claims:

22 A method of operation of a synchronous memory device,
wherein the memory device includes a plurality of memory cells,
the method of operation of the memory device comprises:

23 receiving an external clock signal;

24 receiving first block size information from a bus controller,
wherein the first block size information defines a first amount of
25 data to be output by the memory device onto a bus in response to a
read request;

26 receiving a first request from the bus controller; and

27 outputting the first amount of data corresponding to the first
28 block size information, in response to the first read request, onto the

1 bus synchronously with respect to the external clock signal.

2 Hynix's SDRAMs and DDR SDRAMs satisfy every limitation of claim 18 of the
3 '918 patent when they are operated in a computer system. *See* Section B.1.a, b, c, h, B.3.a.

4 **b. Claim 24**

5 Claim 24 of the '918 patent claims "[t]he method of claim 18 further including
6 storing a delay time code in an access time register, the delay time code being representative of a
7 number of clock cycles to transpire before data is output onto the bus after receipt of a read
8 request and wherein the first amount of data corresponding to the first block size information is
9 output in accordance with the delay time code."

10 Hynix's SDRAMs and DDR SDRAMs meet the additional limitation of claim 24.
11 *See* Section B.2.a, b. The amount of data corresponding to the block size information or burst
12 length is made available after the amount of cycles represented by the CAS latency, that is, in
13 accordance with the delay time code.

14 **c. Claim 33**

15 Claim 33 of the '918 patent claims "[t]he method of claim 18 further including
16 generating at least one internal clock signal using a delay locked loop and the external clock
17 signal wherein the first amount of data corresponding to the first block size information is output
18 onto the bus synchronously with respect to at least one internal clock signal."

19 Hynix's DDR SDRAMs meet the additional limitations of claim 33. *See* Section
20 B.6.a.

21 **4. U.S. Patent No. 6,324,120²⁶**

22 **a. Claim 26**

23 Claim 26 of the '120 patent claims:

24 A synchronous dynamic random access memory device
25 having at least one memory section including a plurality of memory
cells, the memory device comprising:

26 ²⁶ In addition to the claims discussed below, Rambus also moves for summary judgment with
27 respect to claims 1, 5, 6, 7, and 12 of the '120 patent. *See* Murphy Decl. ¶¶ 59-79. These method
28 claims have limitations corresponding essentially to limitations in claims 26, 28, 33, and 34 of the
'120 patent and claim 28 of the '916 patent, *infra*, and infringe for the same reasons when
Hynix's devices are in operation.

1 clock receiver circuitry to receive an external clock signal;

2 input receiver circuitry, including a first plurality of input
3 receivers to sample block size information synchronously with
4 respect to the external clock signal, wherein the block size
5 information defines an amount of data to be output by the memory
6 device in response to a first operation code; and

7 a plurality of output drivers to output the amount of data in
8 response to the first operation code.

9 In the context of claim 26, the “first operation code” signifies a read operation
10 since data is output in response. Hynix’s SDRAMs and DDR SDRAMs then satisfy every
11 limitation of claim 26 of the ’120 patent. *See* Section B.1.a, b, c, g, h, B.3.a., b.

12 **b. Claim 28**

13 Claim 28 is dependent on claim 27 which has not been asserted. Claim 27, in turn,
14 is dependent on claim 26 and adds the limitation that “the amount of data is output synchronously
15 with respect to the external clock signal.” This limitation is satisfied by Hynix’s SDRAMs and
16 DDR SDRAMs. *See* Section B.1.h. Claim 28 adds the additional limitation that “a first portion
17 of the amount of data is output synchronously with respect to a rising edge transition of the
18 external clock signal and a second portion of the amount of data is output synchronously with
19 respect to a falling edge transition of the external clock signal.” This limitation is satisfied by
20 Hynix’s DDR SDRAM devices. *See* Section B.5a.

21 **c. Claim 30**

22 Claim 30 is dependent on claim 29 which has not been asserted. Claim 29, in turn,
23 is dependent on claim 26 and adds the limitation that “the input receiver circuitry samples the first
24 operation code synchronously with respect to the external clock signal.” As noted above, the
25 “first operation code” in the context of claim 26 refers to a read operation; such an operation code
26 is sampled synchronously by the input receivers in SDRAMs and DDR SDRAMs. *See* Section
27 B.1.e. Claim 30 adds the limitation that “the input receiver circuitry includes a second plurality
28 of input receivers to receive the first operation code.” This additional limitation is also met by
Hynix’s SDRAMs and DDR SDRAMs. *See id.*

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d. Claim 33

Claim 33 depends on claim 29 and adds the limitation that “the first operation code includes precharge information.” As noted above, the “first operation code,” for purposes of these claims, refers to a read operation. The code signifying a read operation in Hynix’s SDRAMs and DDR SDRAMs includes precharge information, as required by claim 33. *See* Section B.4.a.

e. Claim 34

Claim 34 depends on claim 26 and adds the limitation that the device further includes “a programmable register to store a value which is representative of a number of clock cycles of the external clock signal to transpire before the memory device outputs the data in response to the first operation code.”

Hynix’s SDRAMs and DDR SDRAMs meet the additional limitation of claim 34. *See* Section B.2.a, b.

f. Claim 38

Claim 38 depends on claim 26 and adds the limitation that the device further includes “delay lock loop circuitry coupled to the clock receiver circuitry to generate an internal clock signal, wherein the plurality of output drivers output data in response to the internal clock signal.”

Hynix’s DDR SDRAMs meet this additional limitation. *See* Section B.6.a.

5. U.S. Patent No. 6,452,863

a. Claim 14

Claim 14 of the ’863 patent claims:

A method of operation in a synchronous memory device, wherein the memory device includes a plurality of memory cells, the method of operation of the memory device comprises:

receiving first block size information from a memory controller, wherein the memory device is capable of processing the first block size information, wherein the first block size information represents a first amount of data to be input by the memory device in response to an operation code;

receiving the operation code, from the memory controller,

1 synchronously with respect to an external clock signal; and
2 inputting the first amount of data in response to the
3 operation code.

4 Claim 14 of the '863 patent is similar to claim 1 of the '120 patent, with the
5 principal difference being that claim 14 relates to writing data to the DRAM as opposed to
6 reading data from the DRAM. Like the operation codes specifying read operations, *see* Section
7 B.1.e, operation codes specifying write operations are inputs to the DRAMs and are received
8 synchronously with respect to the external clock signal. *See* Murphy Decl. ¶ 104. Since “burst
9 length” in Hynix’s SDRAMs and DDR SDRAMs applies to reads and writes, these devices
10 satisfy every limitation of claim 14 when the devices are operated. *See* Sections B.1.a, b, B.3.a,
11 b.

12 **b. Claim 15**

13 Claim 15 of the '863 patent claims “[t]he method of claim 14 wherein inputting
14 the first amount of data includes receiving the first amount of data synchronously with respect to
15 the external clock signal.”

16 Hynix’s SDRAMs and DDR SDRAMs meet this additional limitation since input
17 data, like other inputs to the devices, is received synchronously with respect to the external clock.
18 *See* Section B.1.a.

19 **c. Claim 16**

20 Claim 16 of the '863 claims “[t]he method of claim 15 wherein the first amount of
21 data is sampled over a plurality of clock cycles of the external clock signal.”

22 As discussed above, the “first amount of data” in claim 14 of the '863 patent
23 corresponds to the amount of data specified by the “first block size information,” which, in
24 Hynix’s SDRAMs and DDR SDRAMs corresponds to the burst length stored in the mode
25 register. In Hynix’s SDRAMs, since one bit of data is received per clock cycle, as shown for
26 example in the timing diagram on page 2 of the SDRAM Operation document, the additional
27 limitation of claim 16 will be satisfied whenever the burst length is programmed to be 2 or more.
28 (The possible values are 1, 2, 4, 8 or Full Page. SDRAM Data Sheet at 1.) In Hynix’s DDR

1 SDRAMs, since two bits of data are received per clock cycle, as shown for example in the timing
2 diagram on page 24 of the DDR Data Sheet, the additional limitation of claim 16 will be satisfied
3 whenever the burst length is programmed to be 4 or 8. (The possible values are 2, 4 or 8. DDR
4 Data Sheet at 20.)

5 **6. U.S. Patent No. 6,426,916²⁷**

6 **a. Claim 26**

7 Claim 26 of the '916 patent claims:

8 A synchronous semiconductor memory device having at
9 least one memory section including a plurality of memory cells, the
memory device comprising:

10 clock receiver circuitry to receive an external clock signal;

11 first input receiver circuitry to sample block size
12 information synchronously with respect to the external clock signal,
13 wherein the block size information is representative of an amount
of data to be output by the memory device in response to a first
operation code;

14 a register which stores a value that is representative of an
15 amount of time to transpire after which the memory device outputs
the first amount of data; and

16 a plurality of output drivers to output the amount of data in
17 response to the first operation code and after the amount of time
transpires.

18 In the context of claim 26, the "first operation code" signifies a read
19 operation since data is output in response. Hynix's SDRAMs and DDR SDRAMs
20 then satisfy every limitation of claim 26 of the '916 patent. See Section B.1.a, b, c,
21 g B.2.a, b, B.3.a., b.

22 **b. Claim 28**

23 Claim 28 of the '916 patent claims "[t]he memory device of claim 26 wherein in
24 response to a second operation code, the value is stored in the register."
25

26 ²⁷ In addition to the claims discussed below, Rambus also moves for summary judgment with
27 respect to claims 1, 3, 9, 12, and 14 of the '916 patent. See Murphy Decl. ¶¶ 112-129. These
28 method claims have limitations corresponding essentially to limitations in claims 26, 28 and 31 of
the '916 patent, *infra*, and claim 33 of the '120 patent, *supra*, and infringe for the same reasons
when Hynix's devices are in operation.

1 Hynix's SDRAMs and DDR SDRAMs meet the additional limitation of claim 28.
2 See Section B.2.d.

3 **c. Claim 31**

4 Claim 31 of the '916 patent claims "[t]he memory device of claim 26 wherein a
5 first portion of the amount of data is output synchronously with respect to a rising edge transition
6 of the external clock signal and a second portion of the amount of data is output synchronously
7 with respect to a falling edge transition of the external clock signal."

8 Hynix's DDR SDRAMs meet the additional limitation of claim 31. See Section
9 B.5.a.

10 **d. Claim 37**

11 Claim 37 of the '916 patent claims "[t]he memory device of claim 26 wherein the
12 first input receiver circuitry samples address information synchronously with respect to the
13 external clock signal."

14 Hynix's SDRAMs and DDR SDRAMs meet the additional limitation of claim 37.
15 See Section B.1.f.

16 **e. Claim 40**

17 Claim 40 of the '916 patent claims "[t]he memory device of claim 26 further
18 including delay lock loop circuitry, coupled to the clock receiver circuitry, to generate an internal
19 clock signal, wherein the plurality of output drivers output the amount of data in response to the
20 internal clock signal."

21 Hynix's DDR SDRAMs meet the additional limitations of claim 40. See Section
22 B.6.a.

23 **7. U.S. Patent No. 6,378,020**

24 **a. Claim 30 (not asserted)**

25 Claim 30 of the '020 patent claims:

26 An integrated circuit device comprising:

27 input receiver circuitry to sample an operation code synchronously
28 with respect to a first transition of an external clock signal, the
operation code specifying a read operation; and

1 output driver circuitry to output data in response to the operation
2 code, wherein:

3 the output driver circuitry outputs a first portion of data in response
4 to a rising edge transition of the external clock signal; and
5 the output driver circuitry outputs a second portion of data in
6 response to a falling edge transition of the external clock signal.

7 Although claim 30 has not been asserted, it contains limitations included in the
8 dependent claims, discussed below, which have been asserted. Hynix's DDR SDRAMs satisfy
9 every limitation of claim 30 of the '020 patent. *See* Section B.1.e, g, B.5.a.

10 **b. Claim 31**

11 Claim 31 of the '020 patent claims "[t]he integrated circuit device of claim 30
12 further including a memory array having a plurality of memory cells."

13 Hynix's DDR SDRAMs meet the additional limitation of claim 31. *See* Section
14 B.1.b.

15 **c. Claim 32**

16 Claim 32 of the '020 patent claims "[t]he integrated circuit device of claim 31
17 wherein the input receiver circuitry receives address information synchronously with respect to
18 the external clock signal."

19 Hynix's DDR SDRAMs meet the additional limitation of claim 32. *See* Section
20 B.1.f.

21 **d. Claim 35**

22 Claim 35 of the '020 patent claims "[t]he integrated circuit device of claim 30
23 further including a clock alignment circuit to receive the external clock signal."

24 The parties agree that a "clock alignment circuit" is "a circuit for adjusting the
25 timing relationship between a clock signal and another signal." In DDR SDRAMs, the DLL
26 adjusts the timing relationship between the internal clock signal that it generates and the external
27 clock signal so that that output data is aligned with the external clock signal. Murphy Decl. ¶¶
28 38-40, 158. Therefore, Hynix's DDR SDRAMs meet the additional limitation of claim 35.

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e. Claim 36

Claim 36 of the '020 patent claims "[t]he integrated circuit device of claim 35 wherein the clock alignment circuit generates an internal clock signal, and the output driver circuitry outputs data in response to the internal clock signal."

As noted above, the "clock alignment circuit" corresponds to the DLL in DDR SDRAMs. This DLL generates an internal clock signal in response to which the output driver circuitry outputs data. See Section B.6.a. Therefore, Hynix's DDR SDRAMs meet the additional limitation of claim 36.

f. Claim 38

Claim 38 of the '020 patent claims "[t]he integrated circuit device of claim 30 wherein the rising edge transition of the external clock signal and the falling edge transition of the external clock signal transpire in one clock cycle of the external clock signal."

As the timing diagrams in the DDR Data Sheet make clear, data is output on the rising edge and falling edge of the clock in a single clock cycle. See, e.g., DDR Data Sheet at 24 (timing diagram shows data A0 output on rising edge of clock (CLK) cycle and data A1 output on falling edge of same clock cycle). Therefore, Hynix's DDR SDRAM devices meet the additional limitation of claim 38.

IV. CONCLUSION

For the reasons set forth above, Rambus respectfully requests that the Court grant Rambus summary judgment of infringement with respect to the claims that are the subject of this motion.

DATED: January 27, 2004

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