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UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

HYNIX SEMICONDUCTOR INC., HYNIX SEMICONDUCTOR AMERICA INC., HYNIX SEMICONDUCTOR U.K. LTD., and HYNIX SEMICONDUCTOR DEUTSCHLAND GmbH,

Plaintiffs,

vs.

RAMBUS INC.,

Defendant.

CASE NO. CV 00-20905 RMW

RAMBUS'S SUPPLEMENTAL BRIEF RE CONSTRUCTION OF "SYNCHRONOUS MEMORY DEVICE" AND DEFINITION OF "PACKET"

[Request for Judicial Notice Filed Separately]

On March 24, 2004, at the conclusion of two days of hearings on claim construction issues and the parties' respective motions for summary judgment, the Court indicated that it would allow the parties to submit briefs commenting on the Court's tentative construction of the term "synchronous memory device." In addition, the Court requested that the parties provide a definition of the term "packet." Rambus hereby submits this supplemental brief addressing both of these issues in turn.

I. CONSTRUCTION OF "SYNCHRONOUS MEMORY DEVICE"

On March 24, 2004, after the previous day's hearing on claim construction issues, the Court offered the following tentative construction of "synchronous memory device": "A memory device that receives an external clock to govern the response timing of the memory device operation(s)." This construction may not be sufficiently clear with respect to the term "response timing." To the extent that "response timing" might be argued to refer only to the output timing of the device, the construction should be modified to clarify that input and output timings are both governed by the external clock. Thus, if the Court is not inclined to adopt Rambus's earlier proposed construction, the Court's tentative construction is acceptable but, to be clear, should be modified to read: "A memory device that receives an external clock to govern the timing of input and output operations of the memory device."

This clarification is in accord with the patent specification and the way those skilled in the art use the term "synchronous" in this context. As Hynix concedes, the patent specification discloses a preferred embodiment in which both inputs and outputs are governed by an external clock. *See* Hynix's Responsive Claim Construction Brief at 12 ("The 'memory devices' of this 'system of this invention' [referring to a quote from the specification] recognize address, input data and control signals and transfer output data signals synchronously with respect to an external clock, as required by Rambus's proposed construction.").

Hynix also concedes that certain static RAMs known as synchronous SRAMs that existed prior to the filing of Rambus's patent had their inputs and outputs both governed by an external clock. *See* Hynix's Responsive Claim Construction Brief at 13 ("To be sure, some synchronous SRAMs known prior to the Rambus applications were 'synchronous memory devices' as Rambus

construes the term . . . ."). Likewise, in the accused products at issue in this case, which were named "Synchronous DRAMs" (SDRAMs) to distinguish them from prior art devices that would not be considered synchronous, "inputs *and* outputs are synchronized with the rising edge of the clock input." Declaration of David L. Taylor in Support of Hynix's Motions for Summary Judgment, Ex. 65 (Hynix SDRAM data sheet) at 1 (emphasis added). Further, as presented at the claim construction hearing in this matter, David Johnson, a former Intel engineer whose deposition was noticed by Hynix, testified that in his usage a "synchronous device" has the property that "everything it sent *or* received was off of the clock edges." Johnson Depo. at 79:12 – 80:2 (emphasis added).

By contrast, Hynix has pointed to *no* examples whatsoever of a device being referred to by a person of skill in the art as a "synchronous device" (as opposed to a device that may perform certain operations synchronously with respect to one or more clocks or timing signals) that does not have the timing of both its input *and* output operations governed by an external clock. At the claim construction hearing, Hynix's counsel suggested, for example, that certain "video RAMs," also known as VRAMs should be considered "synchronous" memory devices. Transcript, March 23, 2004, at 51:9 – 54:11 (attached hereto as Exhibit A). While data output was timed by a clock in such VRAMs, other operations, such as the inputting of commands, were performed asynchronously. *Id.* Absent from the record, however, is any evidence of anyone ever referring to such VRAMs as "*synchronous* VRAMs." By contrast, as noted above, SRAMs and DRAMs in which inputs and outputs are governed by an external clock are referred to as "synchronous" SRAMs and "synchronous" DRAMs, respectively.[1]

Rambus respectfully requests that the Court adopt Rambus's proposed construction of "synchronous memory device," which requires that input signals be recognized and output signals

[1] In fact, when memory devices specially designed for video/graphics applications were later introduced that *did* have inputs *and* outputs governed by an external clock, they were designated "*Synchronous* Graphics RAMs" or "SGRAMs," thereby distinguishing them from the previous products, which were called simply "Video RAMs" or "VRAMs." *See* IBM Applications Note, "Understanding VRAM and SGRAM Operation," (Request for Judicial Notice, Ex. 2), at 1 ("Video RAMs (VRAMs) and Synchronous Graphics RAMs (SGRAMs) are DRAMs designed with extra features that make them especially well suited to graphics applications. *VRAM architecture and operation are based on those of the standard DRAM.* SGRAM architecture and operation are based on those of the Synchronous DRAM." (Emphasis added.)).

be transferred in response to an external clock, or, alternatively, modify its tentative construction to read: "A memory device that receives an external clock to govern the timing of input and output operations of the memory device."

II. DEFINITION OF "PACKET"

The Court has requested that the parties define the term "packet." Rambus contends, as it did at the summary judgment hearing, that this term should not be considered to limit any of the asserted claims.[2] Nevertheless, Rambus provides the following explanation of how the term should be understood in the context of the specification of the patents-in-suit.

Around the time of the Rambus patent application, and even today, the term "packet" was most often used in the context of a data communication network involving packet switching – i.e. packets containing data intended for a particular recipient are received at a central location and then "switched" to the appropriate output path depending on their destinations.[3] Indeed, the 1988 IEEE Dictionary, a standard resource for persons of skill in the art, excerpts of which were attached as Exhibit A to the Joint Claim Construction and Prehearing Statement to support Rambus's proposed constructions of a number of terms, defines "packet" only in this context:

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[2] As discussed at the summary judgment hearing, the use of the term "series" by the Federal Circuit in its construction of "read request" creates no limitation of this type. To the contrary, this was simply the term that Rambus itself had used in its Federal Circuit briefing to describe an ordered group of bits transmitted in parallel to the memory device. Rambus had argued to the Federal Circuit, and that court ultimately agreed, that a "read request" in a preferred embodiment of the patents-in-suit was contained in a request packet but was not the entire request packet. Rather, the "read request" in this preferred embodiment corresponded to the "AccessType field" – a four-bit field received in parallel at four pins during the first bus-cycle (half a clock cycle) of the transmission of the packet. *See* Brief of Plaintiff-Appellant Rambus, Inc. (Request for Judicial Notice, Ex. 3) at 17 ("the 'read request' consists of 4 digital 'bits,' called the AccessType field, which are contained within the larger 'request packet.'"); *see also* '263 patent, Figure 4 (indicating that the bits in the AccessType field are received on four parallel "BUSDATA" lines during bus cycle 0). Rambus explained to the Federal Circuit that these four bits constituted "a *series* of 4 digital bits, denominated 0, 1, 2, and 3." Brief of Plaintiff-Appellant Rambus (Request for Judicial Notice, Ex. 3) at 17 n.9. (emphasis added).

Moreover, Hynix apparently concedes that an "operation code," as used in Rambus's claims, need not be sent in a packet. Transcript, March 23, 2004, at 88-89 ("But I think that, that the proper way, or the best way to construe this is that these bits do have to be part of a packet, okay, *or that they have to be sent from, in this case, the master to the memory in some sort of format, whether they're, whether they're done in a sequence or -- probably a sequence, or it could be all done simultaneously.*" (Emphasis added.)).

[3] Typically, a packet in a data communications network (such as the Internet) will be directed through several switches that are used to route the packet to its final destination.

> **packet (data communication).** A group of binary digits including data and control elements which is switched and transmitted as a composite whole. The data and control elements and possibly error control information are arranged in a specified format.

IEEE Standard Dictionary of Electrical and Electronics Terms 663 (4th ed. 1988) (Request for Judicial Notice, Ex. 4).

The IEEE definition can be easily adjusted to remove limitations peculiar to the data communication field and to fit the way a person of skill in the art would use the term "packet" in a more general context, which is the case in the patents at issue. First, the binary digits (commonly referred to as "bits") in a packet need not consist of data and control elements together. As Hynix has indicated, a packet may contain data alone. *See, e.g.*, Hynix's Responsive Claim Construction Brief at 3 ("After a specified amount of time, data to be written to memory or data read from memory was sent over the bus in a separate packet.").[4] Moreover, for purposes of the patents-in-suit, as made clear in the patent specification, a packet need not include data and may include other types of information, such as address information. *See, e.g.*, '263 patent, col. 6:50-52 (noting that a request packet in a preferred embodiment contains "a sequence of bytes comprising address and control information"). Additionally, outside of the data communications context, the packets are transmitted but need not, in general, be "switched" from a particular input path to one of several possible output paths. These observations lead to a definition that captures what one of skill in the art would have meant by the term "packet" when adapted from the packet-switching network context to a more general context, such as the patents-in-suit. The key attributes of a "packet" in this more general context are (1) that it consist of binary digits or bits, (2) that the bits be transmitted as a composite whole (thereby distinguishing

[4] To the extent that Hynix asserts, as it has in its summary judgment briefs, that the definition of "packet" should include a requirement that the packet be transmitted over multiple clock cycles, the example of data packets shows that this is not the case. In a preferred embodiment in the patent specification, "block size" can be set in such a way as to request one byte (i.e. 8 bits) of data. '263 patent, col. 11:37-47 (example of block size encoding indicating that if the BlockSize field is set to 1, one byte of data is to be returned). In this case, in the preferred embodiment in which the bus has 8 data lines, the reply packet containing the 8 bits of data would be returned in one bus cycle (half a clock cycle in a preferred embodiment).

parts of a packet from the packet as a whole), and (3) that the bits be arranged in a specified format (that is, that the positioning of the bits within the packet be required to follow certain rules). Consequently, Rambus proposes the following definition for "packet":

packet. A group of bits that is transmitted as a composite whole.

The bits are arranged in a specified format.

III. CONCLUSION

For the reasons set forth above, Rambus requests that the Court adopt Rambus's proposed construction of the term "synchronous memory device," or, alternatively, modify its tentative construction to read: "A memory device that receives an external clock to govern the timing of input and output operations of the memory device."

Rambus submits that a "packet," in the context of the patents-in-suit, while not a limitation on the asserted claims, should be defined as: "A group of bits that is transmitted as a composite whole. The bits are arranged in a specified format."

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